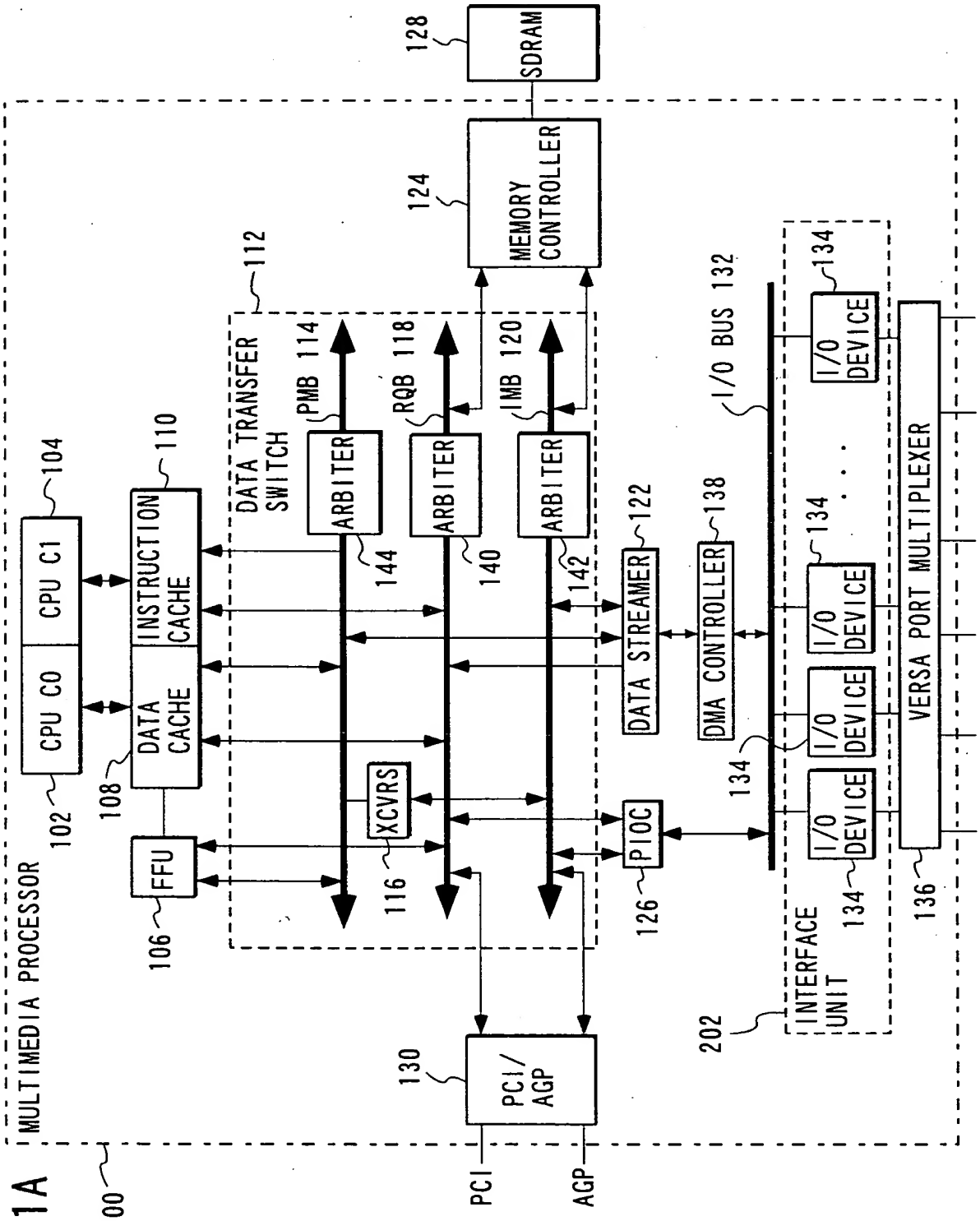

MULTIMEDIA PROCESSOR
100
CPU C0
CPU C1
102
104
DATA CACHE
INSTRUCTION CACHE
108
110
FFU
106
DATA TRANSFER SWITCH
112
PMB 114
RQB 118
IMB 120
ARBITER
ARBITER
ARBITER
144
140
142
XCVRS
116
PIOC
126
DATA STREAMER
122
DMA CONTROLLER
138
MEMORY CONTROLLER
124
SDRAM
128
PCI/ AGP
130
PCI
AGP
I/O BUS 132
I/O DEVICE
I/O DEVICE
I/O DEVICE
I/O DEVICE
134
134
134
134
INTERFACE UNIT
202
VERSA PORT MULTIPLEXER
136

FIG. 1A

FIG. 1B

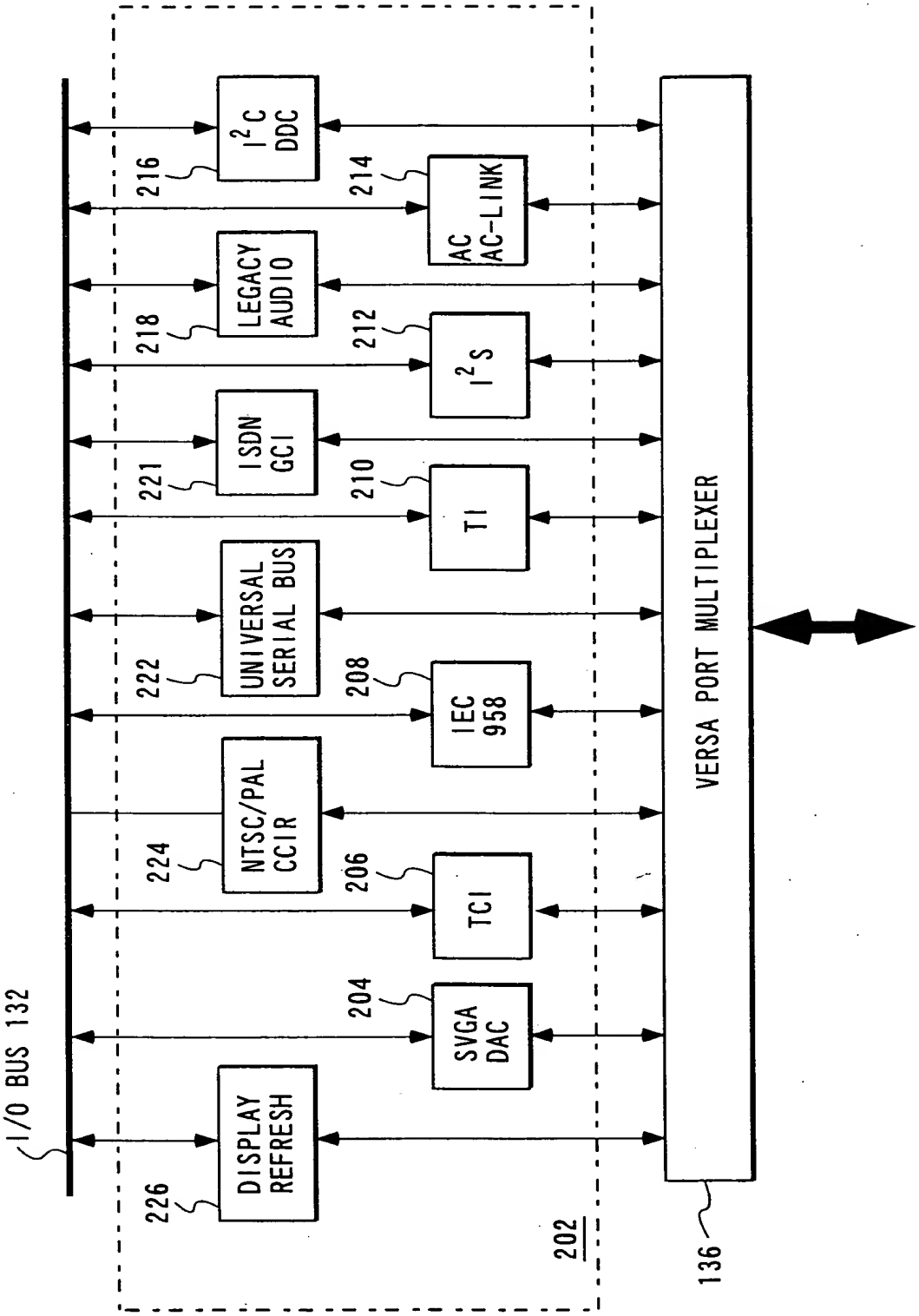

I/O BUS 132
DISPLAY REFRESH
226
SVGA DAC
204
TCI
206
NTSC/PAL CCIR
224
IEC 958
208
UNIVERSAL SERIAL BUS
222
TI
210
ISDN GCI
221
I²S
212
LEGACY AUDIO
218
AC AC-LINK
214
I²C DDC
216
202
VERSA PORT MULTIPLEXER
136

FIG. 1C

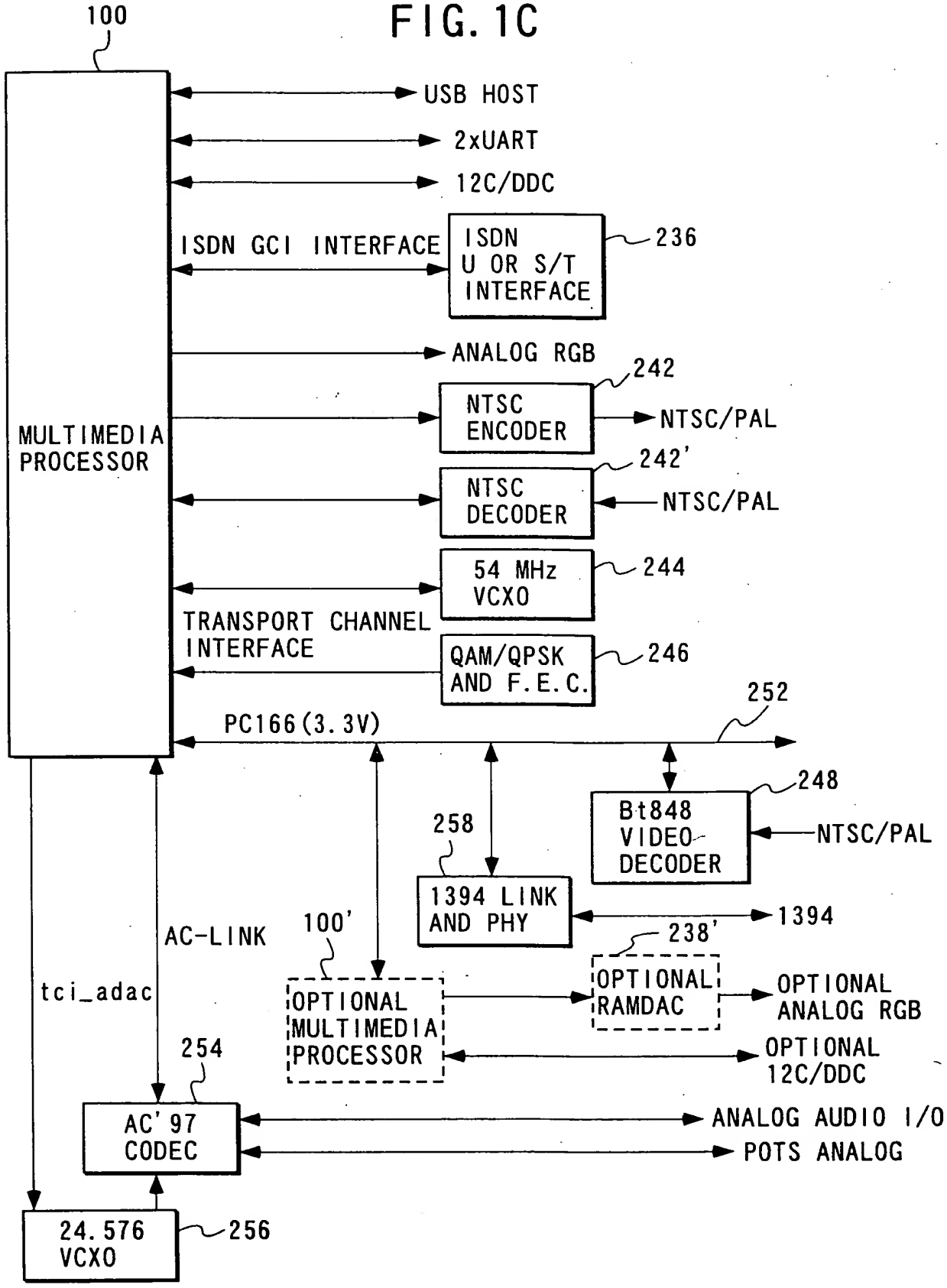

100
MULTIMEDIA PROCESSOR
USB HOST
2xUART
12C/DDC
ISDN GCI INTERFACE
ISDN U OR S/T INTERFACE
236
ANALOG RGB
242
NTSC ENCODER
NTSC/PAL
242'
NTSC DECODER
NTSC/PAL
54 MHz VCXO
244
TRANSPORT CHANNEL INTERFACE
QAM/QPSK AND F.E.C.
246
252
PC166(3.3V)
248
Bt848 VIDEO DECODER
NTSC/PAL
258
1394 LINK AND PHY
1394
AC-LINK
100'
238'
OPTIONAL RAMDAC
OPTIONAL ANALOG RGB
tci_adac
OPTIONAL MULTIMEDIA PROCESSOR
OPTIONAL 12C/DDC
254
AC'97 CODEC
ANALOG AUDIO I/O
POTS ANALOG
24.576 VCXO
256

FIG. 1D

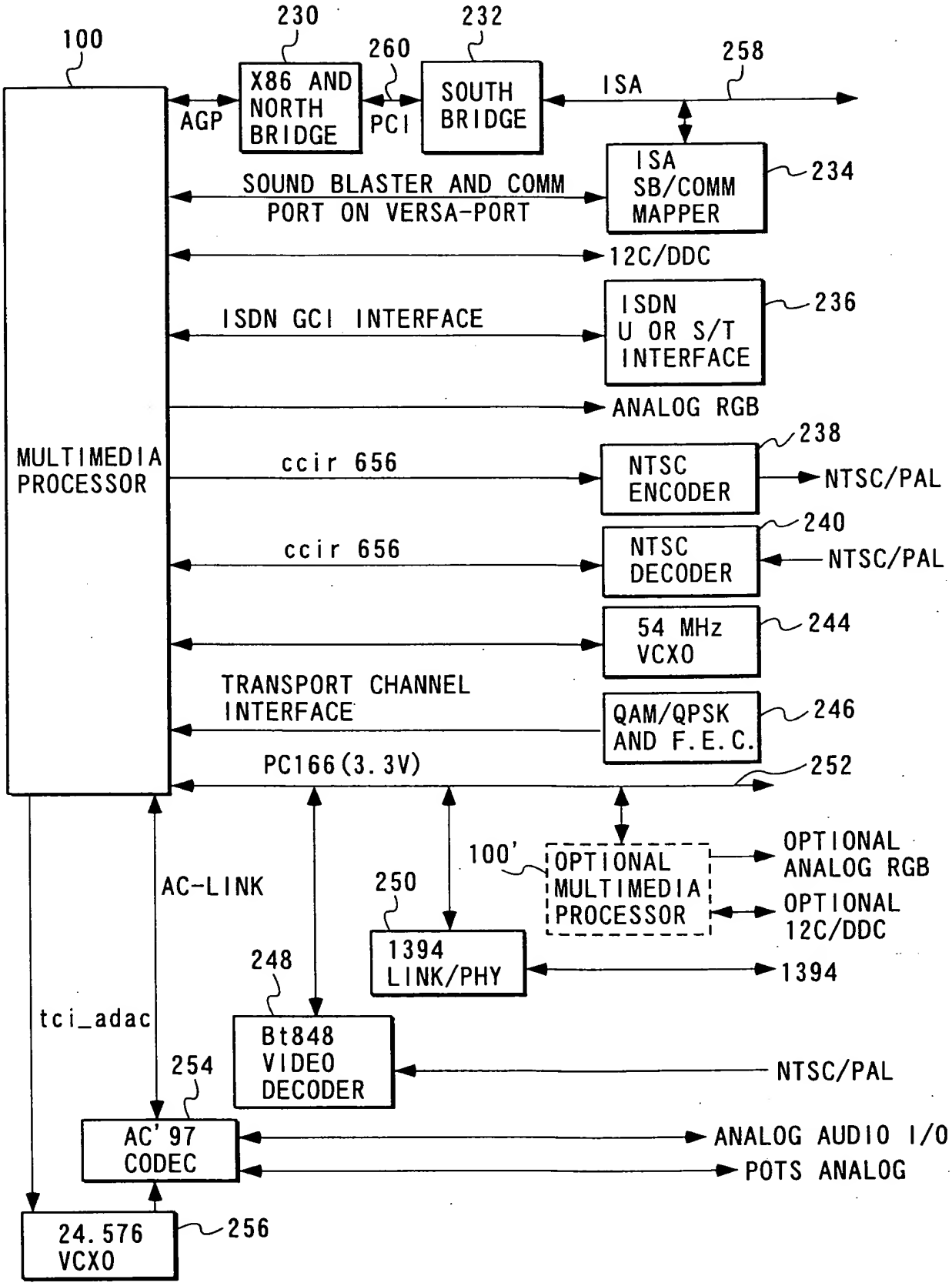

100
230
232
260
258
X86 AND NORTH BRIDGE
SOUTH BRIDGE
AGP
PCI
ISA
ISA SB/COMM MAPPER
234
SOUND BLASTER AND COMM PORT ON VERSA-PORT
I2C/DDC
ISDN GCI INTERFACE
ISDN U OR S/T INTERFACE
236
ANALOG RGB
MULTIMEDIA PROCESSOR
ccir 656
NTSC ENCODER
238
NTSC/PAL
ccir 656
NTSC DECODER
240
NTSC/PAL
54 MHz VCXO
244
TRANSPORT CHANNEL INTERFACE
QAM/QPSK AND F.E.C.
246
PC166(3.3V)
252
100'
OPTIONAL MULTIMEDIA PROCESSOR
OPTIONAL ANALOG RGB
OPTIONAL I2C/DDC
AC-LINK
250
1394 LINK/PHY
1394
248
tci_adac
Bt848 VIDEO DECODER
NTSC/PAL
254
AC'97 CODEC
ANALOG AUDIO I/O
POTS ANALOG
24.576 VCXO
256

FIG. 2

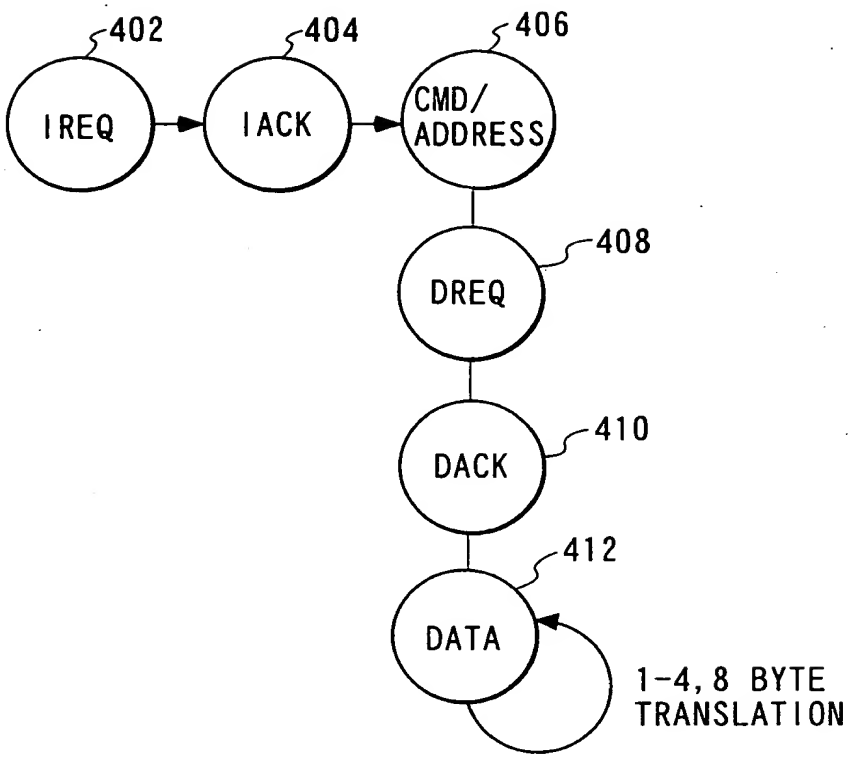


FIG. 3A

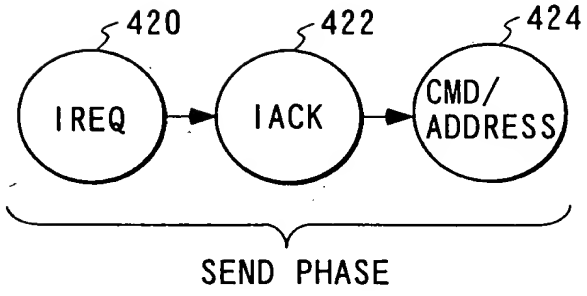


FIG. 3B

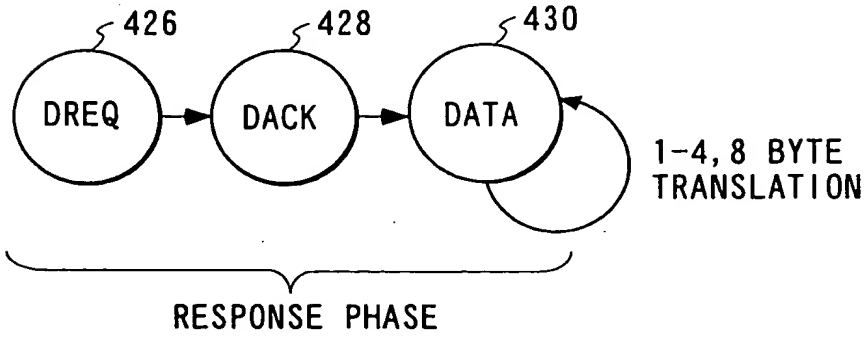


FIG. 4A

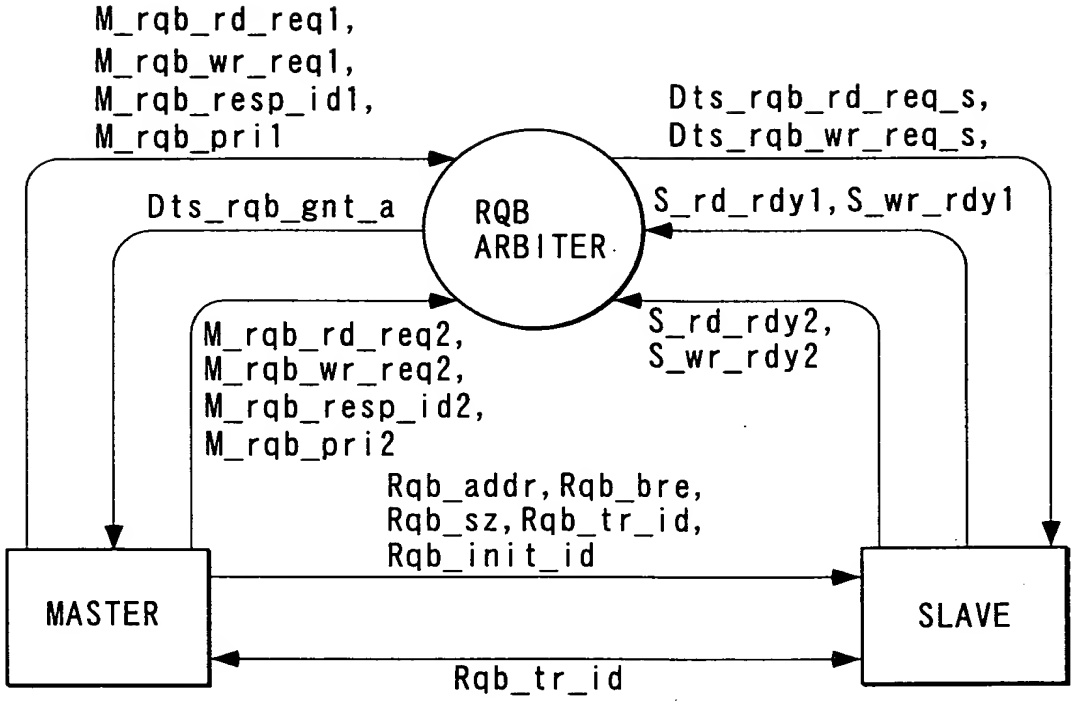

M_rqb_rd_req1,
M_rqb_wr_req1,
M_rqb_resp_id1,
M_rqb_pri1
Dts_rqb_rd_req_s,
Dts_rqb_wr_req_s,
Dts_rqb_gnt_a
RQB
ARBITER
S_rd_rdy1, S_wr_rdy1
S_rd_rdy2,
S_wr_rdy2
M_rqb_rd_req2,
M_rqb_wr_req2,
M_rqb_resp_id2,
M_rqb_pri2
Rqb_addr, Rqb_bre,
Rqb_sz, Rqb_tr_id,
Rqb_init_id
MASTER
SLAVE
Rqb_tr_id

FIG. 4B

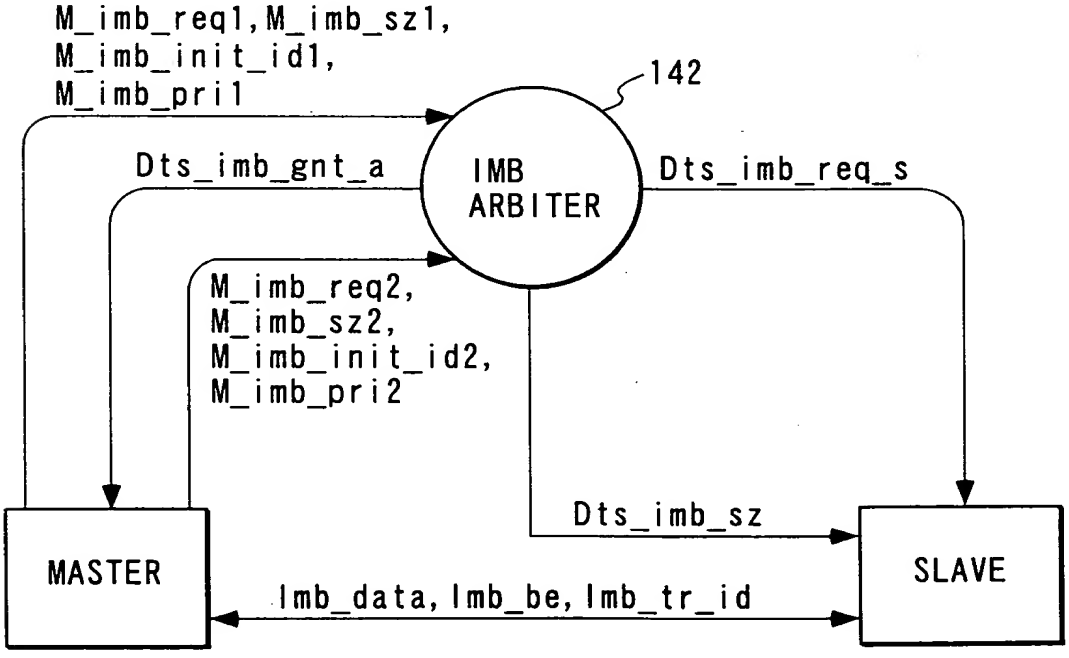

M_imb_req1, M_imb_sz1,
M_imb_init_id1,
M_imb_pri1
142
Dts_imb_gnt_a
IMB
ARBITER
Dts_imb_req_s
M_imb_req2,
M_imb_sz2,
M_imb_init_id2,
M_imb_pri2
Dts_imb_sz
MASTER
SLAVE
Imb_data, Imb_be, Imb_tr_id

FIG. 5A

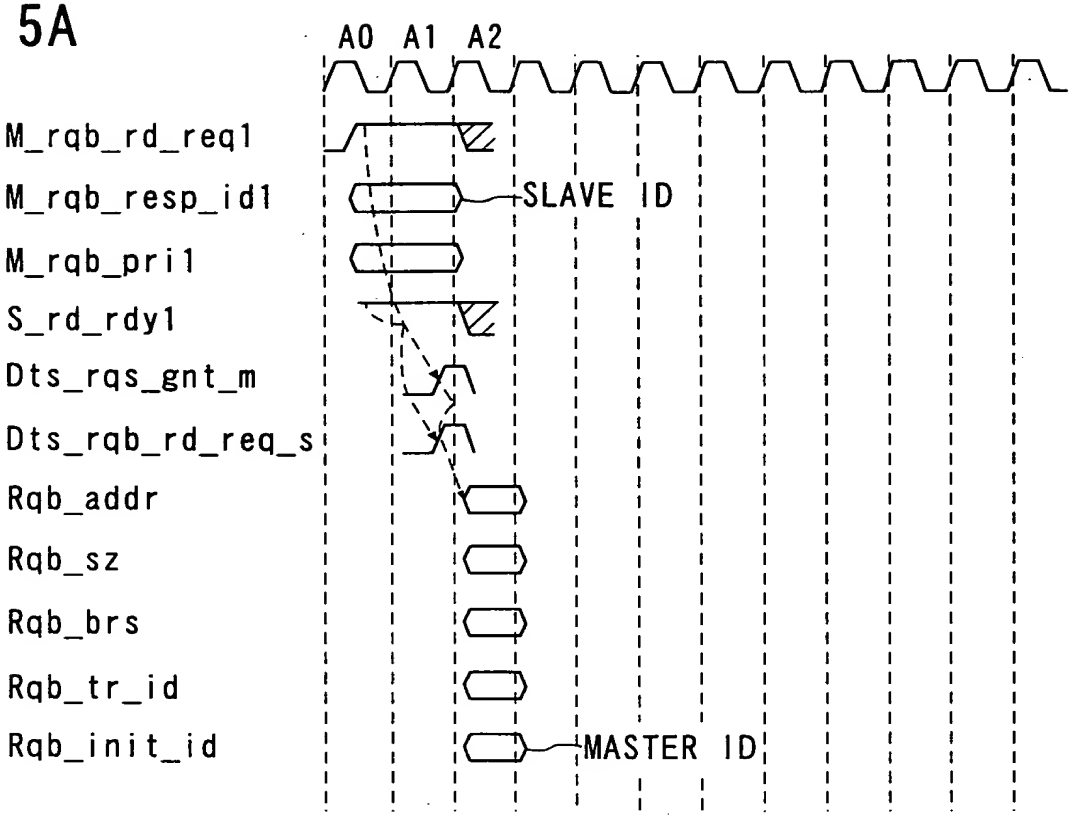
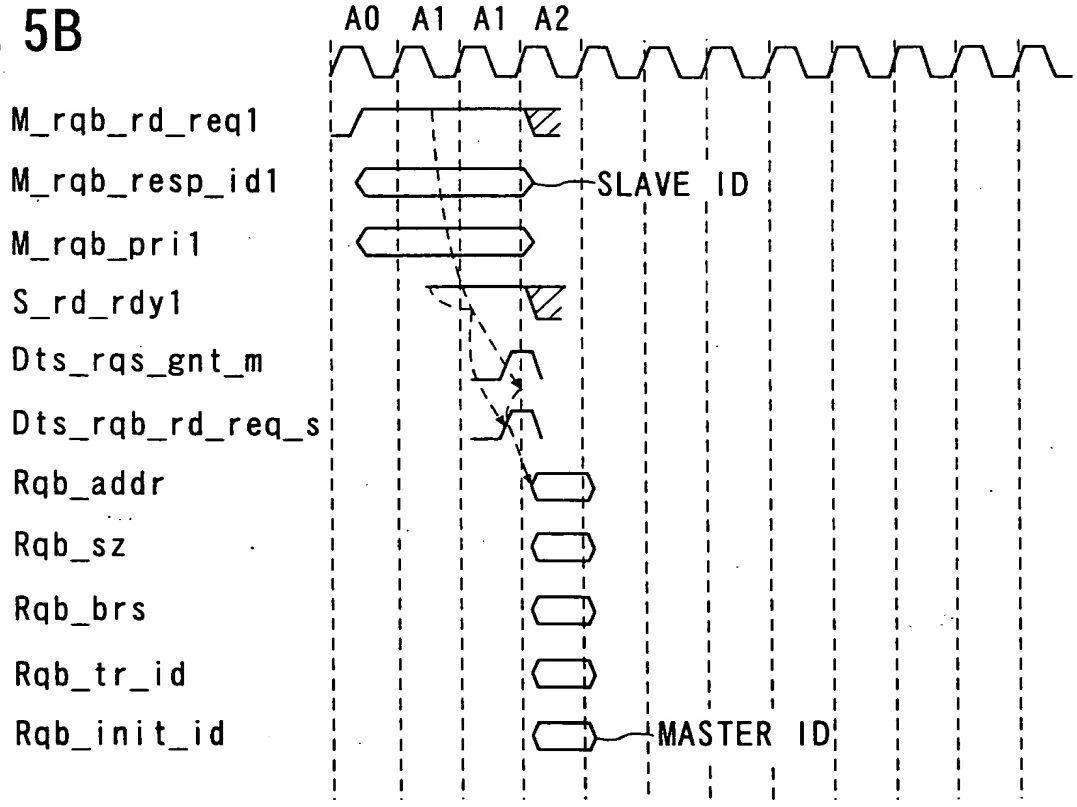


FIG. 5B



EP 1 550 950 A2 20050706

FIG. 5C

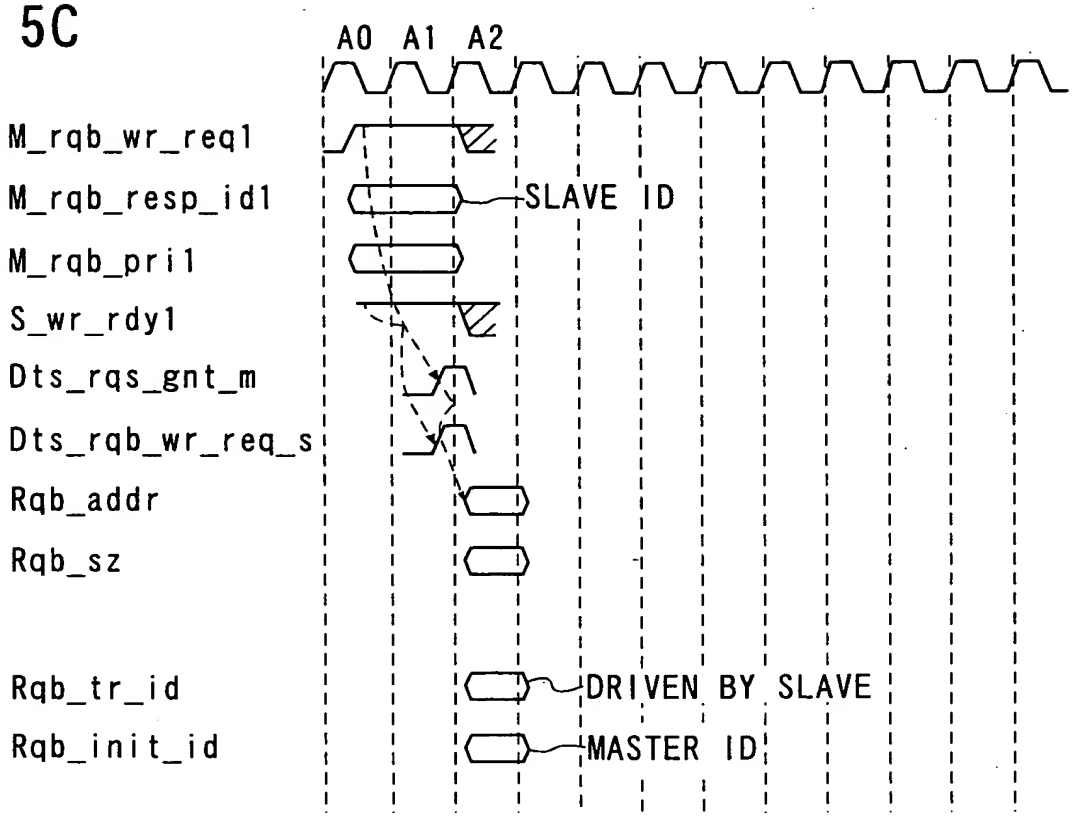

A0 A1 A2
M_rqb_wr_req1
M_rqb_resp_id1
SLAVE ID
M_rqb_pri1
S_wr_rdy1
Dts_rqs_gnt_m
Dts_rqb_wr_req_s
Rqb_addr
Rqb_sz
Rqb_tr_id
DRIVEN BY SLAVE
Rqb_init_id
MASTER ID

FIG. 5D

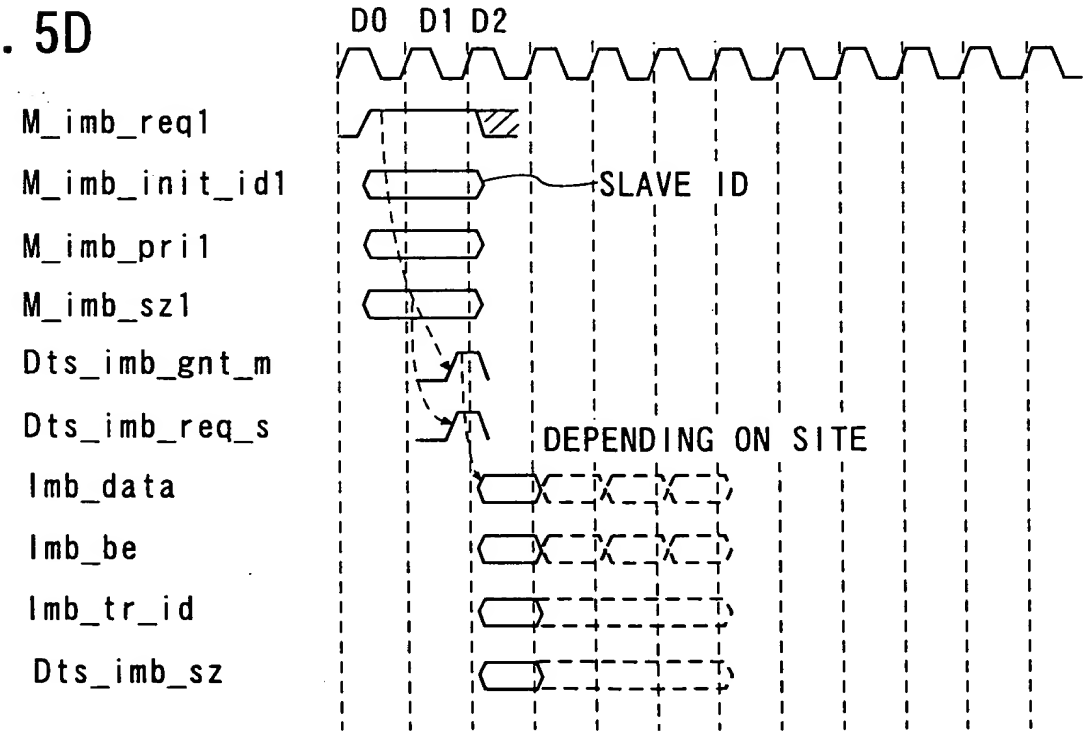

D0 D1 D2
M_imb_req1
M_imb_init_id1
SLAVE ID
M_imb_pri1
M_imb_sz1
Dts_imb_gnt_m
Dts_imb_req_s
DEPENDING ON SITE
Imb_data
Imb_be
Imb_tr_id
Dts_imb_sz

FIG. 6A

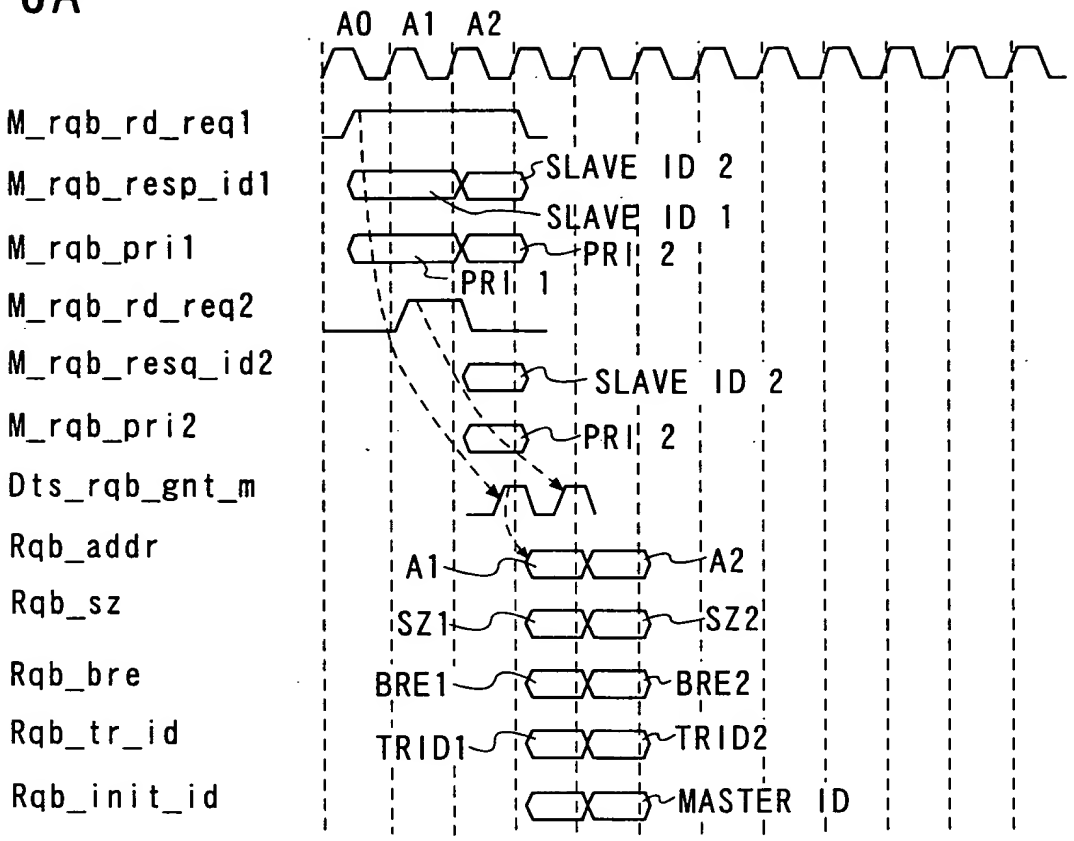

A0 A1 A2
M_rqb_rd_req1
M_rqb_resp_id1
M_rqb_pri1
M_rqb_rd_req2
M_rqb_resq_id2
M_rqb_pri2
Dts_rqb_gnt_m
Rqb_addr
Rqb_sz
Rqb_bre
Rqb_tr_id
Rqb_init_id
SLAVE ID 2
SLAVE ID 1
PRI 2
PRI 1
SLAVE ID 2
PRI 2
A1
A2
SZ1
SZ2
BRE1
BRE2
TRID1
TRID2
MASTER ID

FIG. 6B

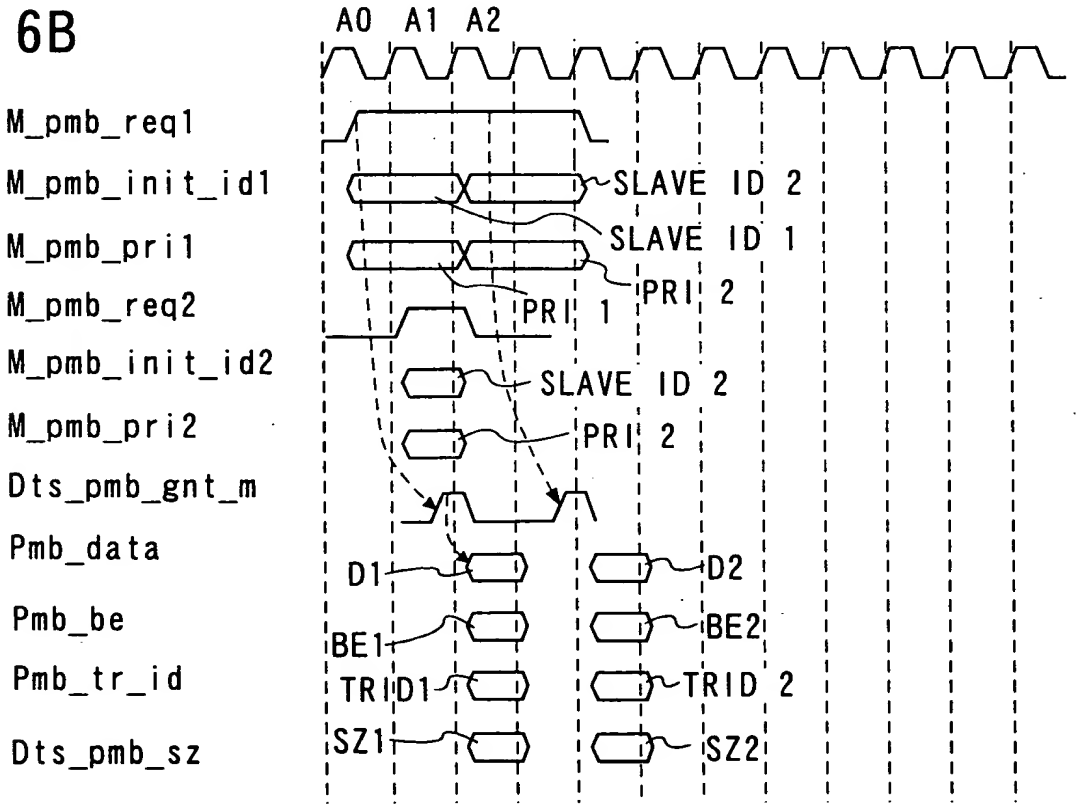

A0 A1 A2
M_pmb_req1
M_pmb_init_id1
M_pmb_pri1
M_pmb_req2
M_pmb_init_id2
M_pmb_pri2
Dts_pmb_gnt_m
Pmb_data
Pmb_be
Pmb_tr_id
Dts_pmb_sz
SLAVE ID 2
SLAVE ID 1
PRI 2
PRI 1
SLAVE ID 2
PRI 2
D1
D2
BE1
BE2
TRID1
TRID 2
SZ1
SZ2

FIG. 6C

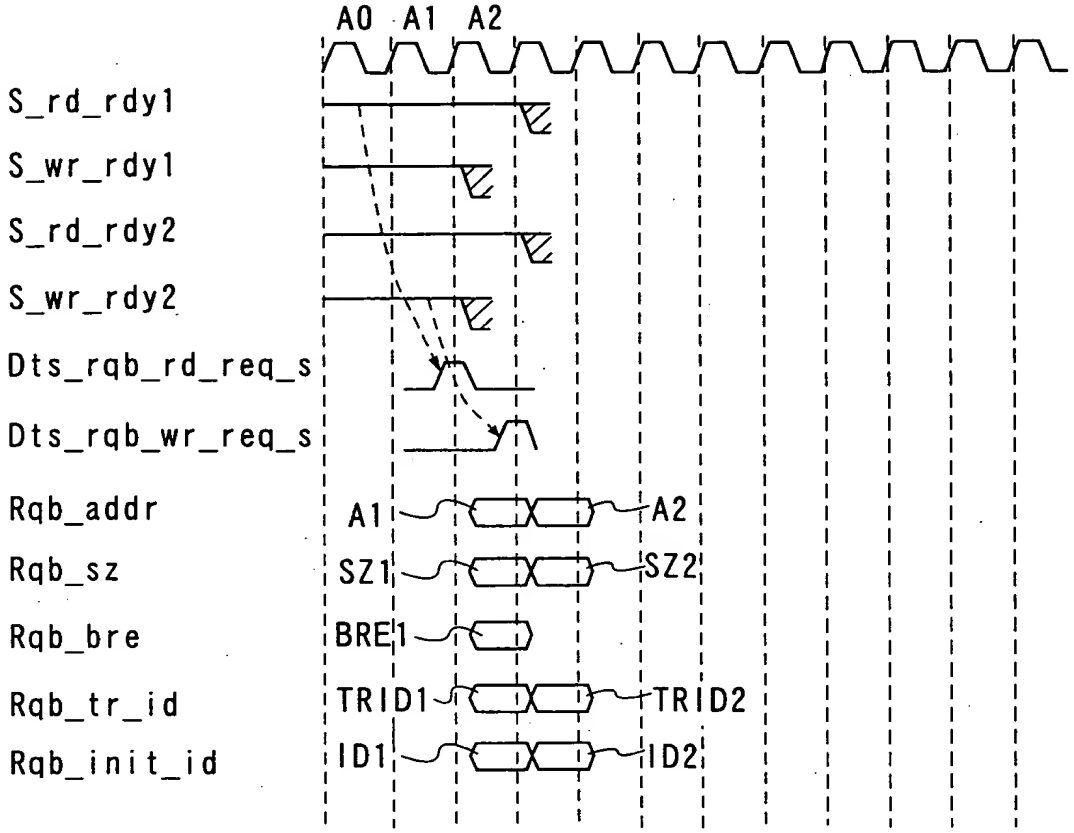

A0
A1
A2
S_rd_rdy1
S_wr_rdy1
S_rd_rdy2
S_wr_rdy2
Dts_rqb_rd_req_s
Dts_rqb_wr_req_s
Rqb_addr
A1
A2
Rqb_sz
SZ1
SZ2
Rqb_bre
BRE1
Rqb_tr_id
TRID1
TRID2
Rqb_init_id
ID1
ID2

FIG. 7

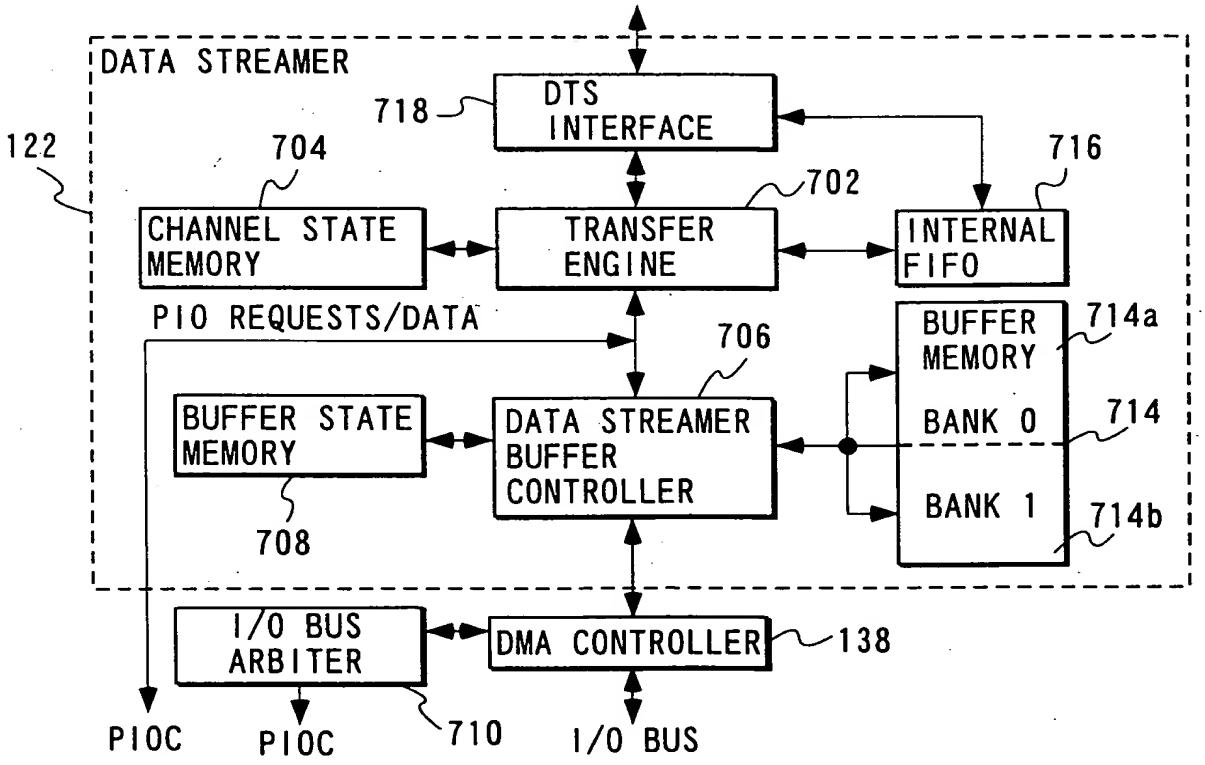

DATA STREAMER
122
718
DTS INTERFACE
704
716
702
CHANNEL STATE MEMORY
TRANSFER ENGINE
INTERNAL FIFO
PIO REQUESTS/DATA
706
BUFFER MEMORY
714a
BUFFER STATE MEMORY
DATA STREAMER BUFFER CONTROLLER
BANK 0
714
BANK 1
714b
708
I/O BUS ARBITER
DMA CONTROLLER
138
PIOC
PIOC
710
I/O BUS

FIG. 8

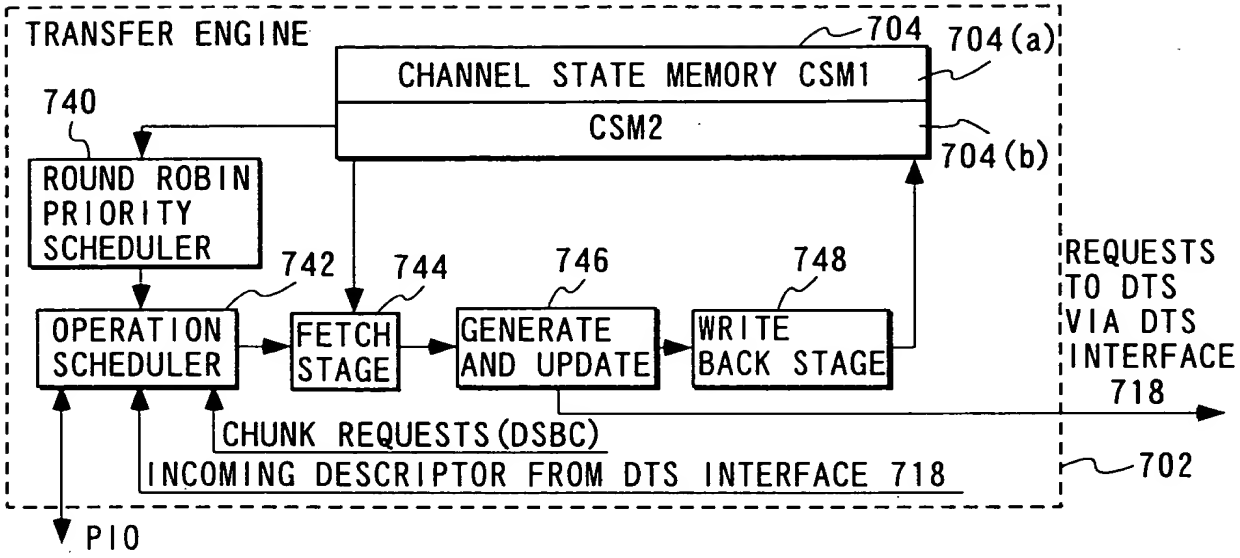

TRANSFER ENGINE
704
704(a)
CHANNEL STATE MEMORY CSM1
CSM2
704(b)
740
ROUND ROBIN PRIORITY SCHEDULER
742
744
746
748
OPERATION SCHEDULER
FETCH STAGE
GENERATE AND UPDATE
WRITE BACK STAGE
REQUESTS TO DTS VIA DTS INTERFACE 718
CHUNK REQUESTS(DSBC)
INCOMING DESCRIPTOR FROM DTS INTERFACE 718
702
PIO

FIG. 9

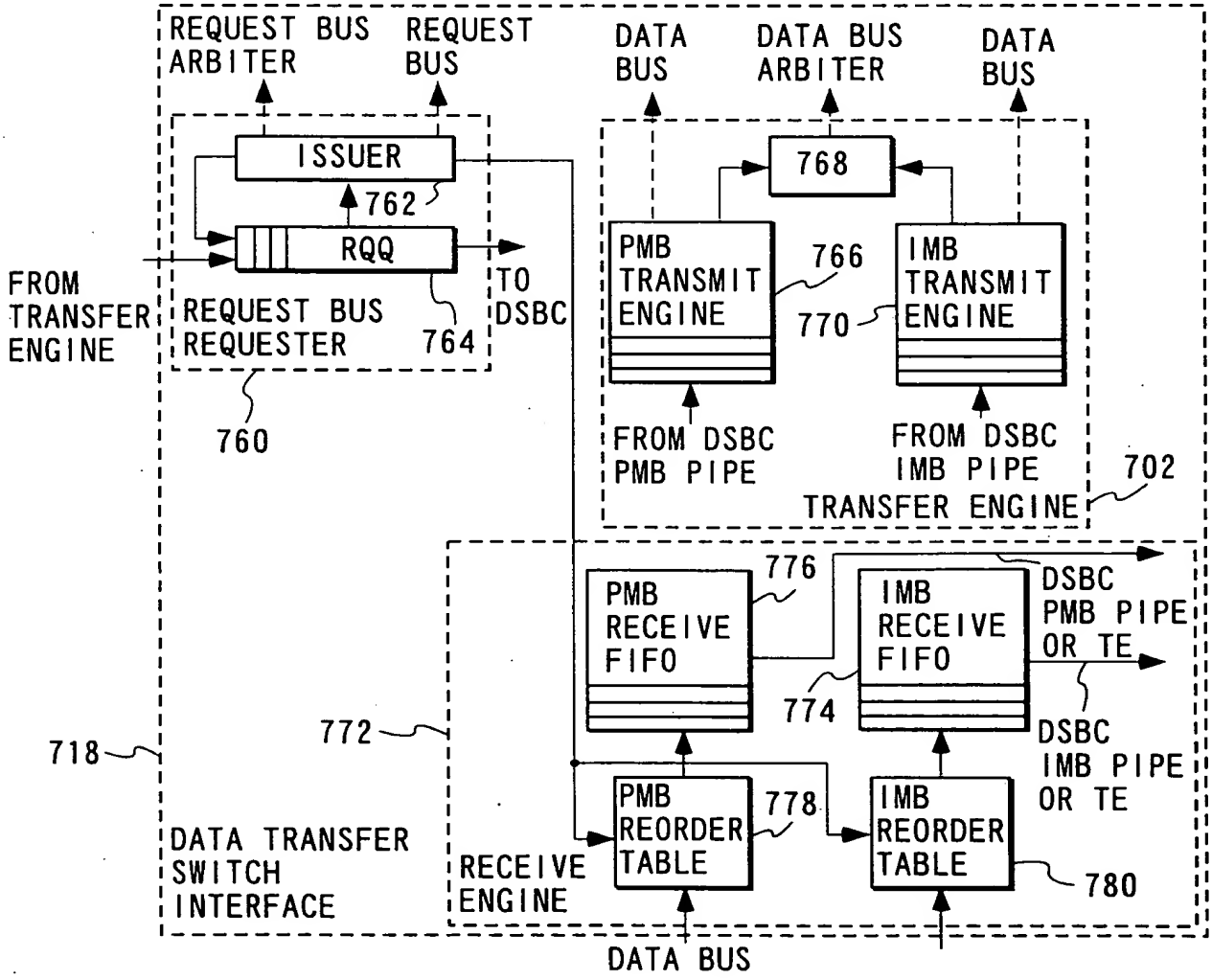

REQUEST BUS ARBITER
REQUEST BUS
DATA BUS
DATA BUS ARBITER
DATA BUS
ISSUER
762
RQQ
FROM TRANSFER ENGINE
REQUEST BUS REQUESTER
764
TO DSBC
760
768
PMB TRANSMIT ENGINE
766
IMB TRANSMIT ENGINE
770
FROM DSBC PMB PIPE
FROM DSBC IMB PIPE
TRANSFER ENGINE
702
776
PMB RECEIVE FIFO
IMB RECEIVE FIFO
DSBC PMB PIPE OR TE
774
DSBC IMB PIPE OR TE
772
718
PMB REORDER TABLE
778
IMB REORDER TABLE
780
DATA TRANSFER SWITCH INTERFACE
RECEIVE ENGINE
DATA BUS

FIG. 10

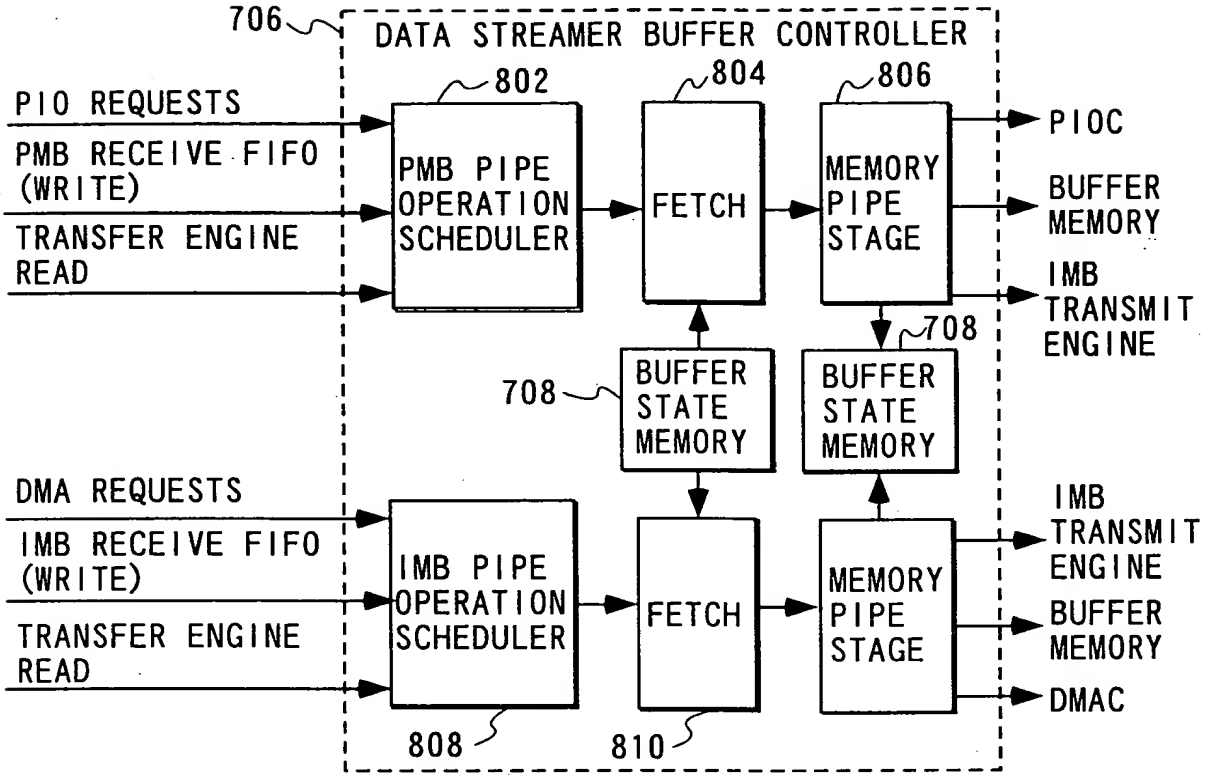

706
DATA STREAMER BUFFER CONTROLLER
802
804
806
PIO REQUESTS
PMB RECEIVE FIFO (WRITE)
TRANSFER ENGINE READ
PMB PIPE OPERATION SCHEDULER
FETCH
MEMORY PIPE STAGE
PIOC
BUFFER MEMORY
IMB TRANSMIT ENGINE
708
708
BUFFER STATE MEMORY
BUFFER STATE MEMORY
DMA REQUESTS
IMB RECEIVE FIFO (WRITE)
TRANSFER ENGINE READ
IMB PIPE OPERATION SCHEDULER
FETCH
MEMORY PIPE STAGE
IMB TRANSMIT ENGINE
BUFFER MEMORY
DMAC
808
810

FIG. 11

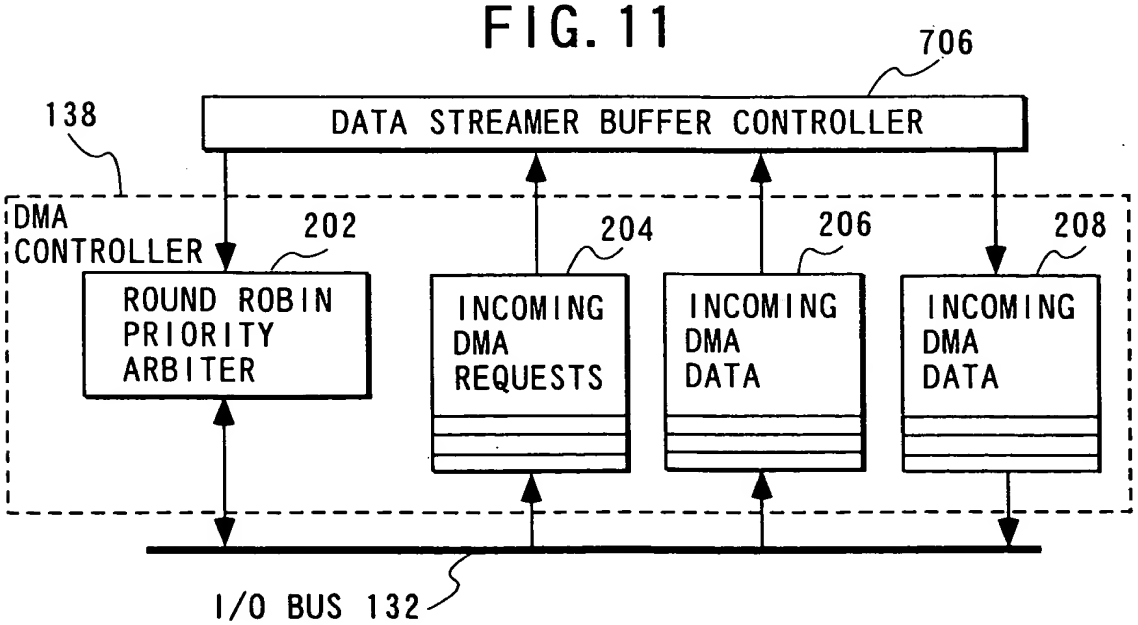

706
138
DATA STREAMER BUFFER CONTROLLER
DMA CONTROLLER
202
204
206
208
ROUND ROBIN PRIORITY ARBITER
INCOMING DMA REQUESTS
INCOMING DMA DATA
INCOMING DMA DATA
I/O BUS 132

FIG. 12

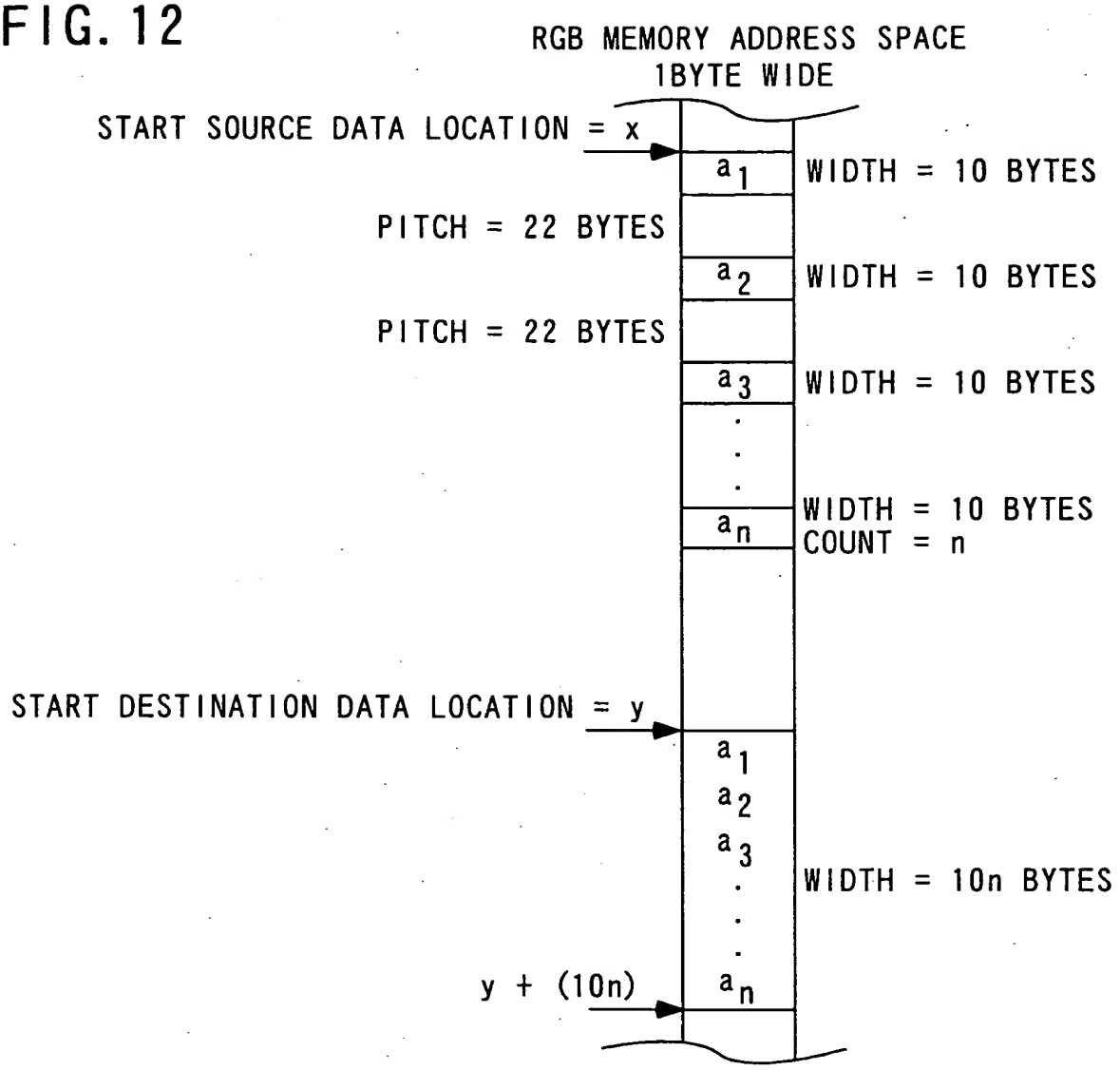

RGB MEMORY ADDRESS SPACE
1BYTE WIDE
START SOURCE DATA LOCATION = x
a1
WIDTH = 10 BYTES
PITCH = 22 BYTES
a2
WIDTH = 10 BYTES
PITCH = 22 BYTES
a3
WIDTH = 10 BYTES
an
WIDTH = 10 BYTES
COUNT = n
START DESTINATION DATA LOCATION = y
a1
a2
a3
WIDTH = 10n BYTES
y + (10n)
an

FIG. 13

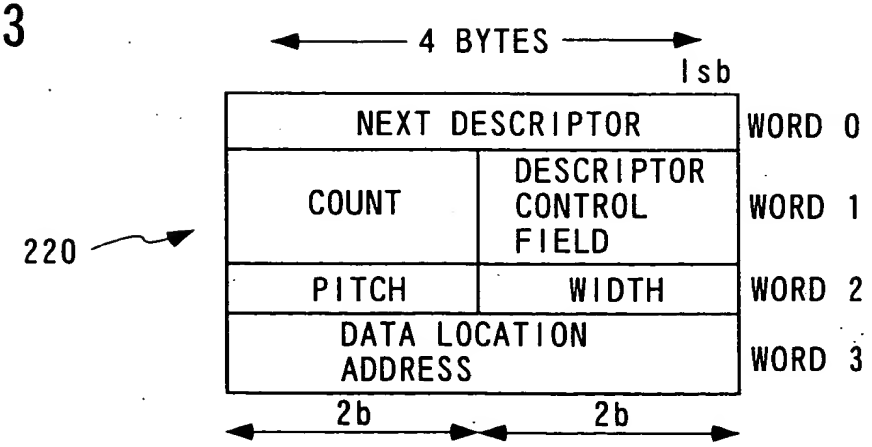

4 BYTES
lsb
NEXT DESCRIPTOR
WORD 0
COUNT
DESCRIPTOR CONTROL FIELD
WORD 1
220
PITCH
WIDTH
WORD 2
DATA LOCATION ADDRESS
WORD 3
2b
2b

FIG. 14

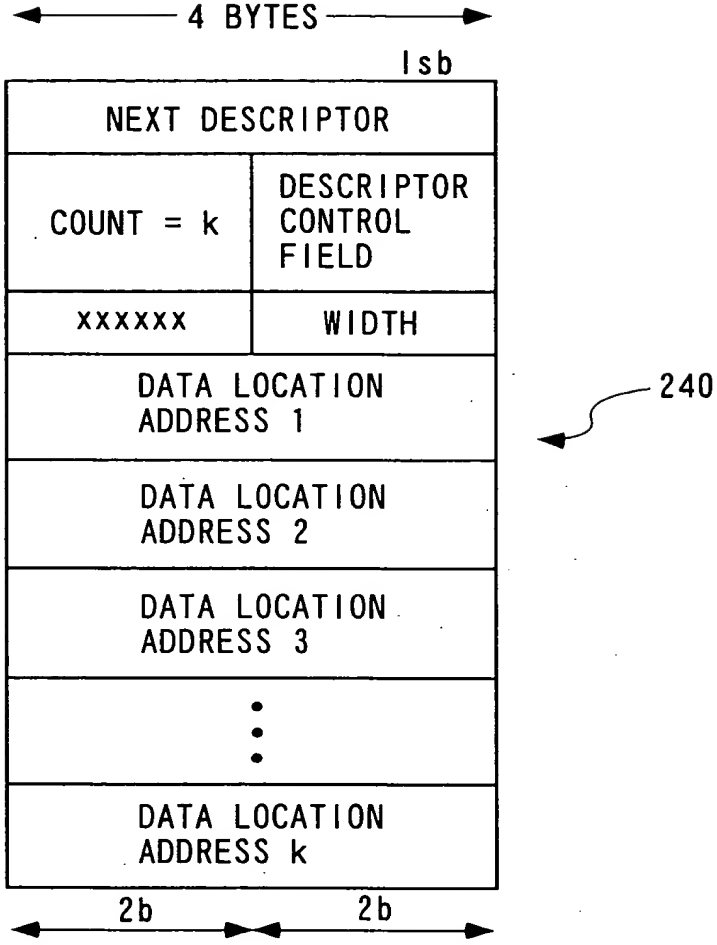

4 BYTES
lsb
NEXT DESCRIPTOR
COUNT = k
DESCRIPTOR CONTROL FIELD
xxxxxx
WIDTH
DATA LOCATION ADDRESS 1
DATA LOCATION ADDRESS 2
DATA LOCATION ADDRESS 3
DATA LOCATION ADDRESS k
240
2b
2b

FIG. 15A

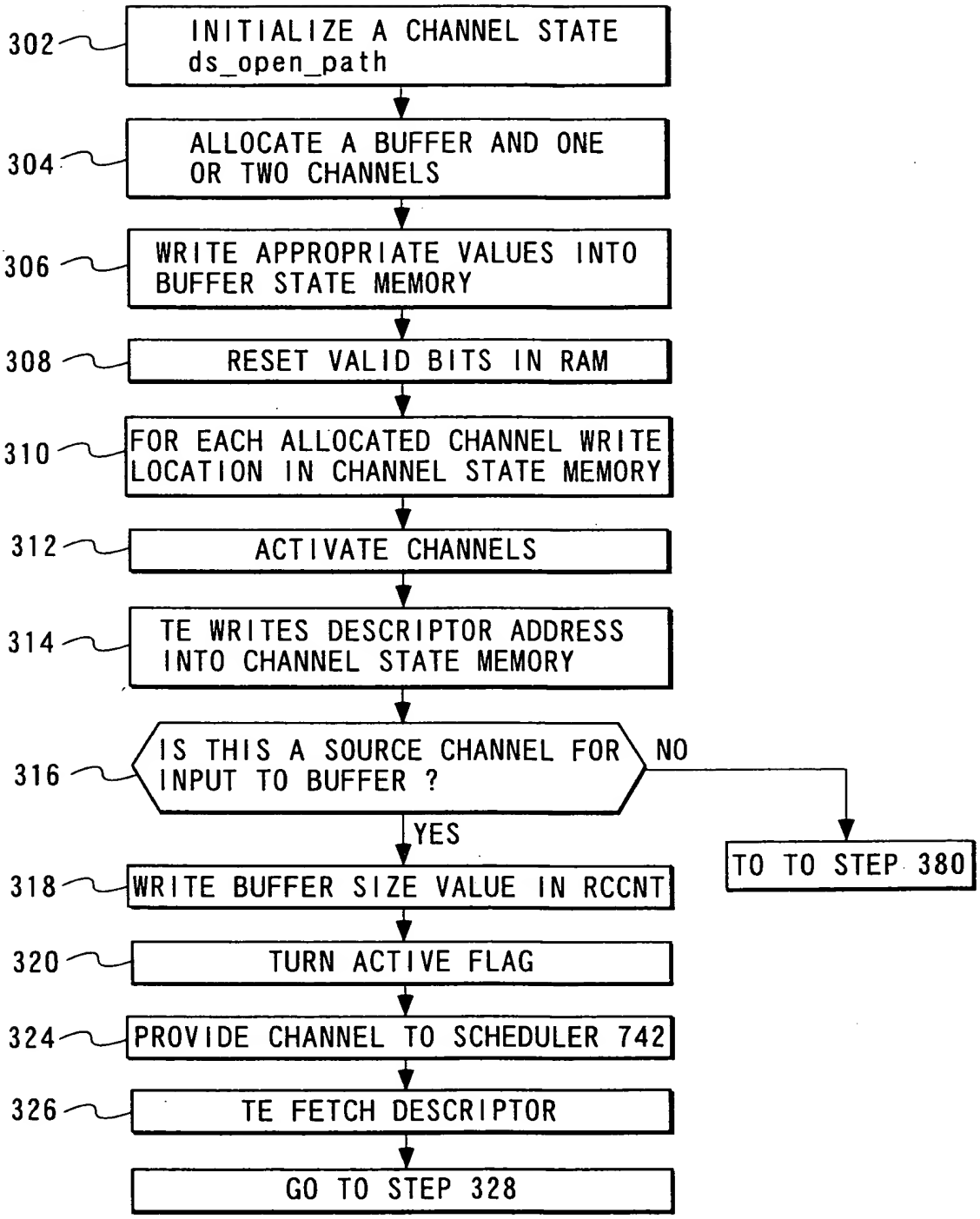

302
INITIALIZE A CHANNEL STATE ds_open_path
304
ALLOCATE A BUFFER AND ONE OR TWO CHANNELS
306
WRITE APPROPRIATE VALUES INTO BUFFER STATE MEMORY
308
RESET VALID BITS IN RAM
310
FOR EACH ALLOCATED CHANNEL WRITE LOCATION IN CHANNEL STATE MEMORY
312
ACTIVATE CHANNELS
314
TE WRITES DESCRIPTOR ADDRESS INTO CHANNEL STATE MEMORY
316
IS THIS A SOURCE CHANNEL FOR INPUT TO BUFFER ?
NO
TO TO STEP 380
YES
318
WRITE BUFFER SIZE VALUE IN RCCNT
320
TURN ACTIVE FLAG
324
PROVIDE CHANNEL TO SCHEDULER 742
326
TE FETCH DESCRIPTOR
GO TO STEP 328

FIG. 15B

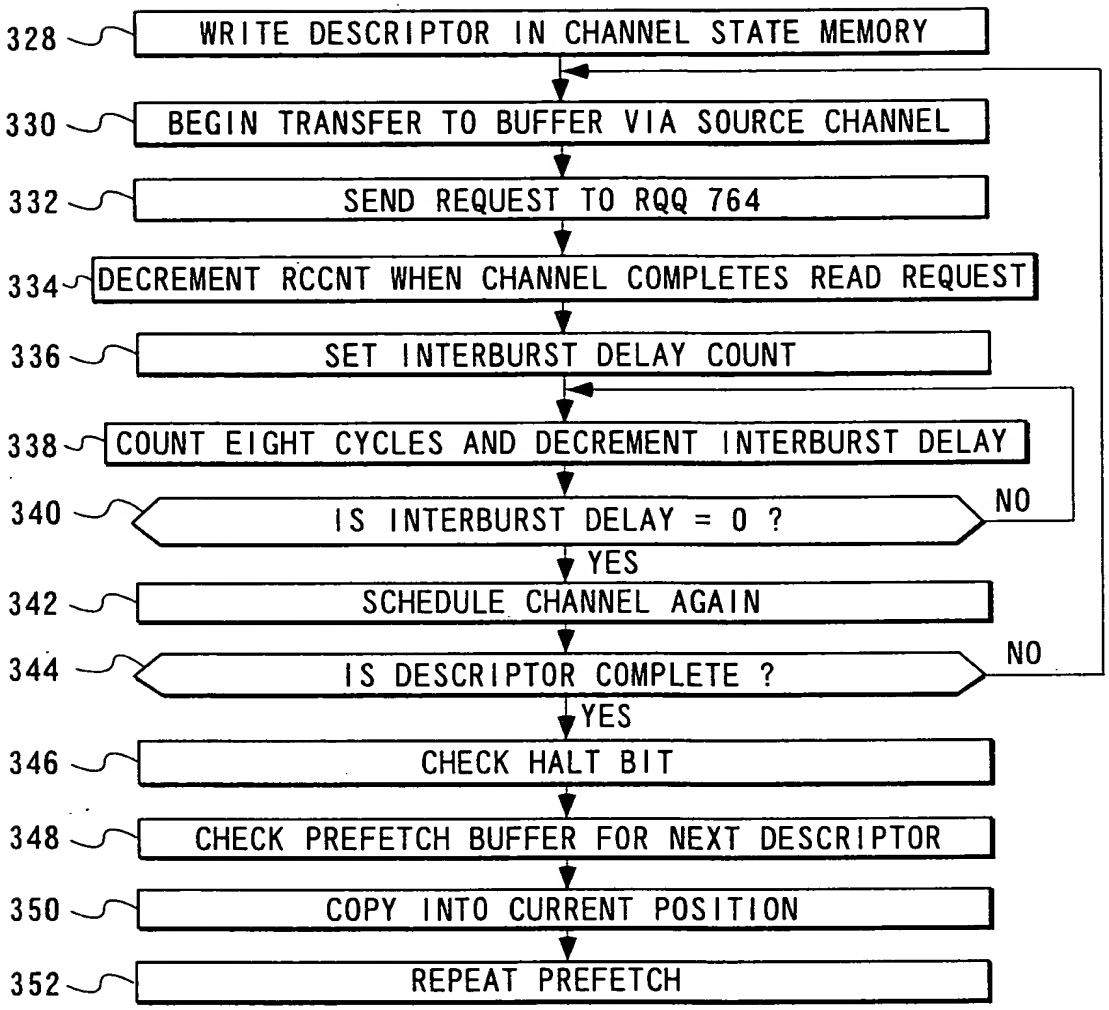


FIG. 15C

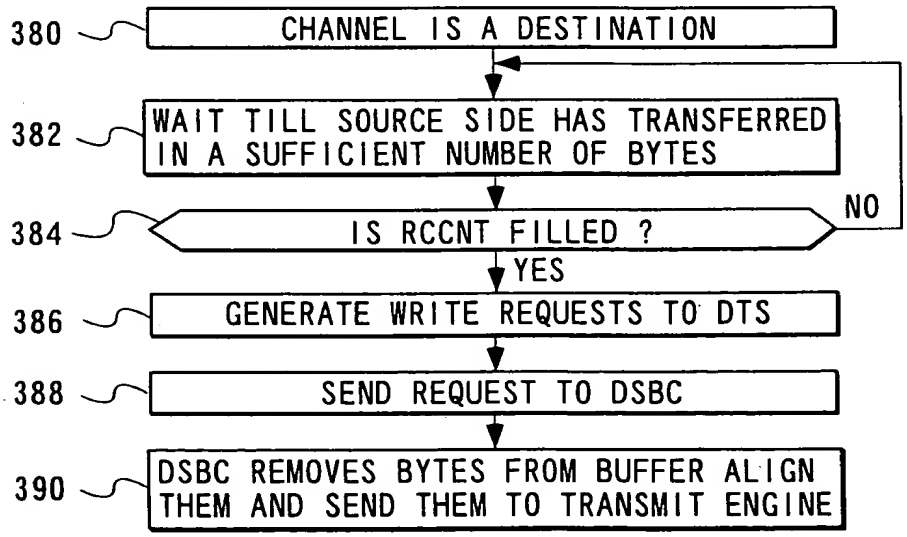


FIG. 16
PIROR ART

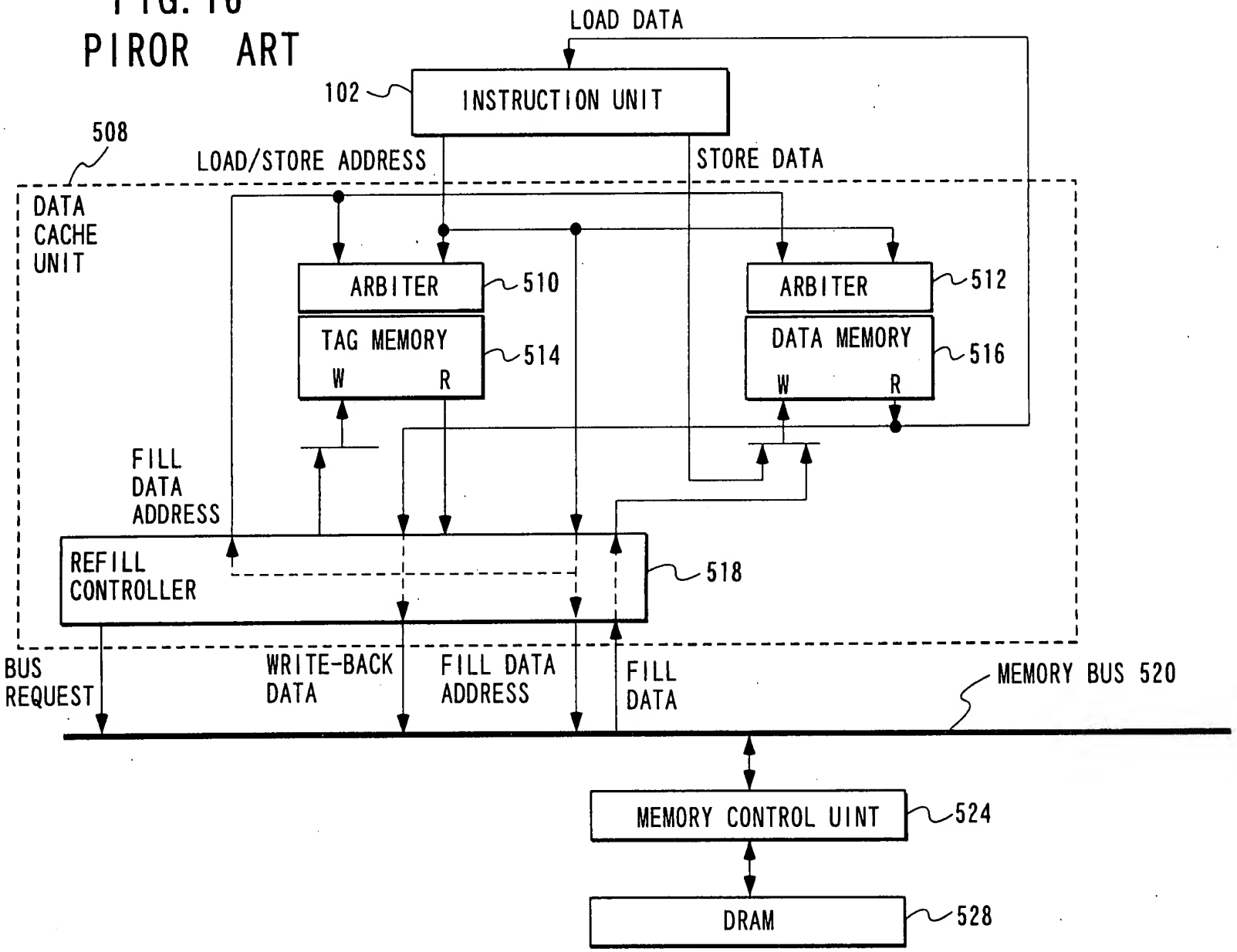


FIG. 17

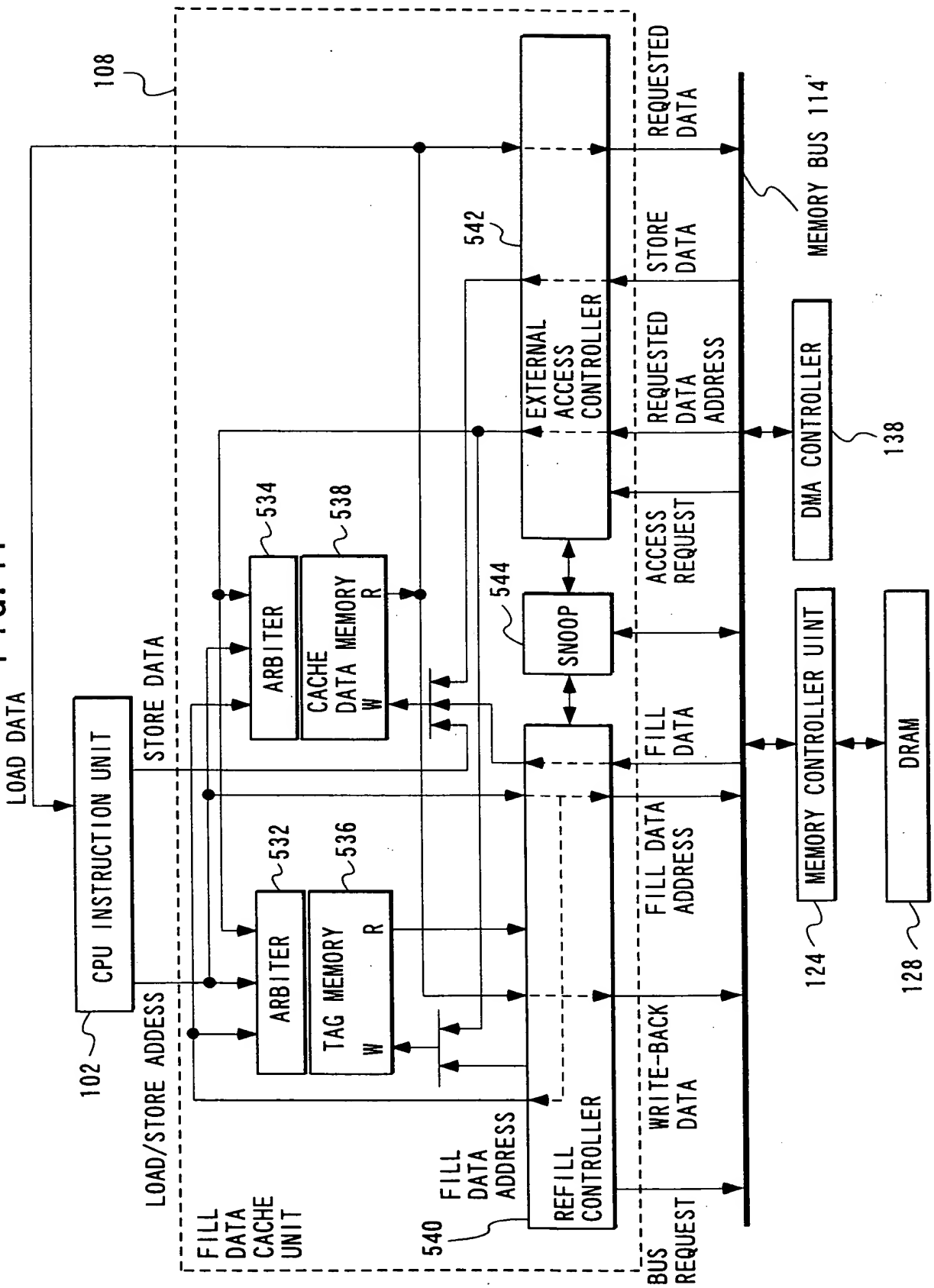

108
LOAD DATA
STORE DATA
CPU INSTRUCTION UNIT
102
LOAD/STORE ADDESS
FILL DATA CACHE UNIT
ARBITER
532
TAG MEMORY
W
R
536
ARBITER
534
CACHE DATA MEMORY
W
R
538
542
EXTERNAL ACCESS CONTROLLER
544
SNOOP
ACCESS REQUEST
REQUESTED DATA ADDRESS
STORE DATA
REQUESTED DATA
FILL DATA
FILL DATA ADDRESS
WRITE-BACK DATA
FILL DATA ADDRESS
540
REFILL CONTROLLER
BUS REQUEST
MEMORY BUS 114'
DMA CONTROLLER
138
MEMORY CONTROLLER UINT
124
DRAM
128

FIG. 18

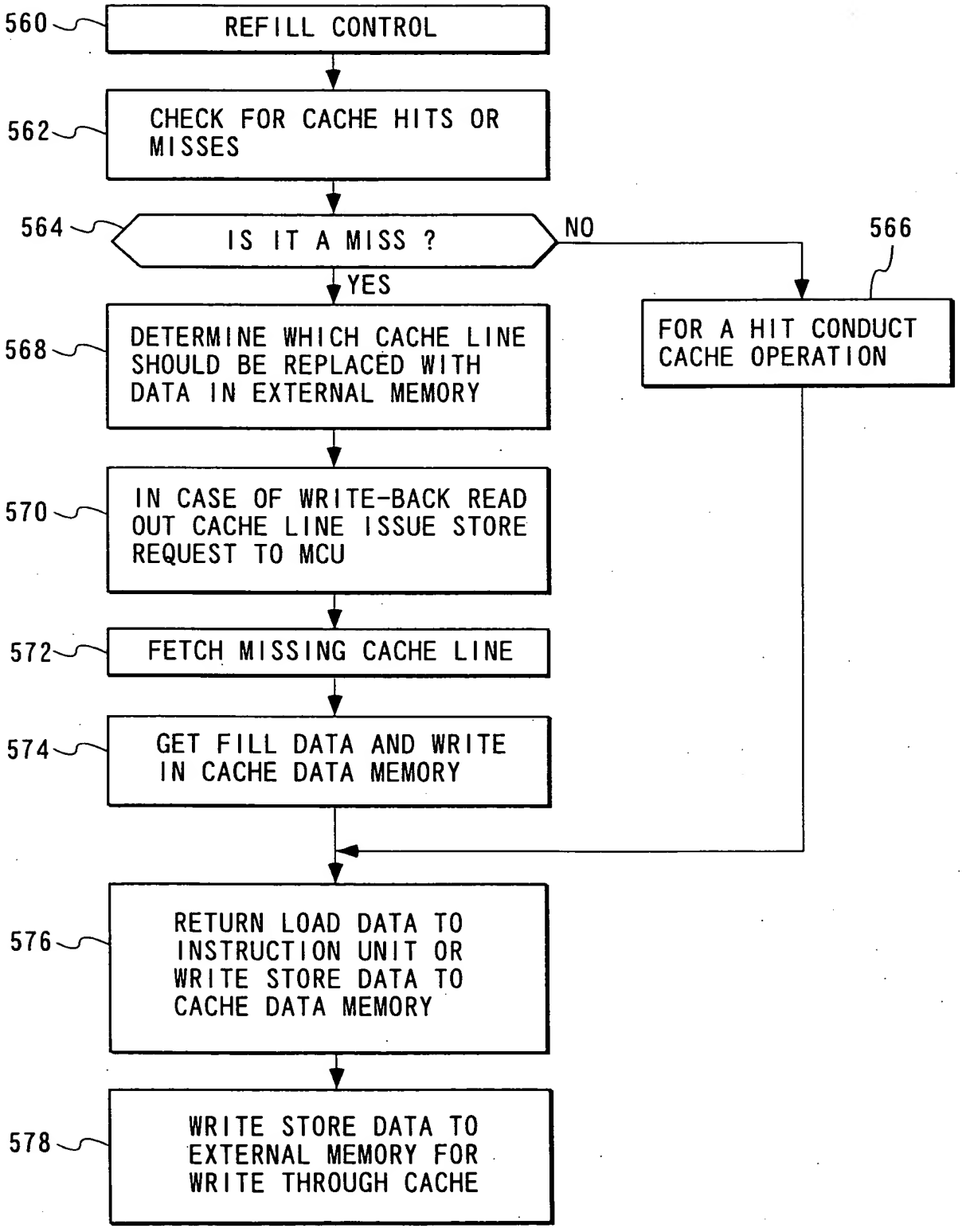

560
REFILL CONTROL
562
CHECK FOR CACHE HITS OR MISSES
564
IS IT A MISS ?
NO
566
FOR A HIT CONDUCT CACHE OPERATION
YES
568
DETERMINE WHICH CACHE LINE SHOULD BE REPLACED WITH DATA IN EXTERNAL MEMORY
570
IN CASE OF WRITE-BACK READ OUT CACHE LINE ISSUE STORE REQUEST TO MCU
572
FETCH MISSING CACHE LINE
574
GET FILL DATA AND WRITE IN CACHE DATA MEMORY
576
RETURN LOAD DATA TO INSTRUCTION UNIT OR WRITE STORE DATA TO CACHE DATA MEMORY
578
WRITE STORE DATA TO EXTERNAL MEMORY FOR WRITE THROUGH CACHE

FIG. 19

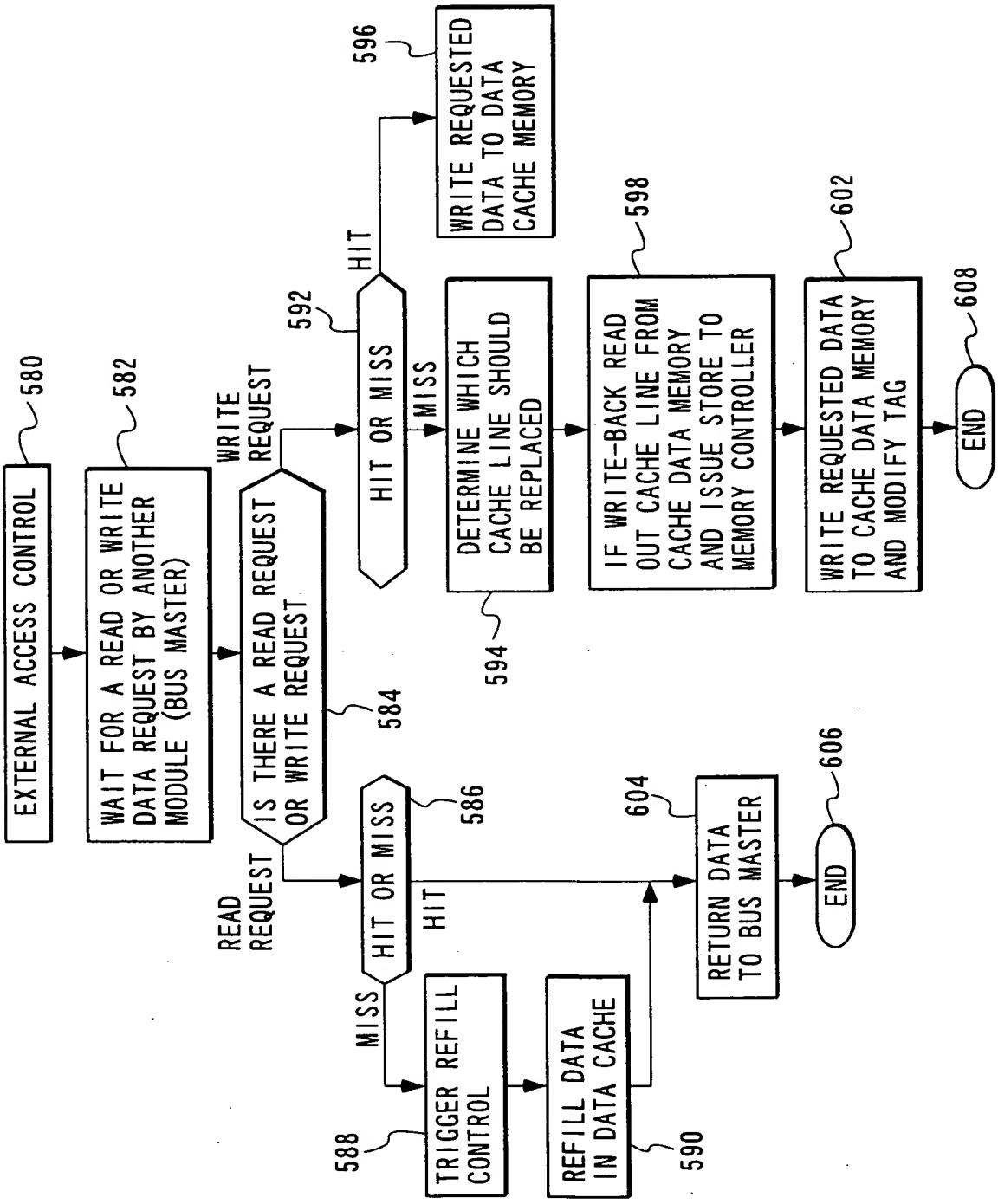

EXTERNAL ACCESS CONTROL
580
WAIT FOR A READ OR WRITE DATA REQUEST BY ANOTHER MODULE (BUS MASTER)
582
IS THERE A READ REQUEST OR WRITE REQUEST
584
READ REQUEST
WRITE REQUEST
HIT OR MISS
586
MISS
HIT
TRIGGER REFILL CONTROL
588
REFILL DATA IN DATA CACHE
590
HIT OR MISS
592
HIT
MISS
WRITE REQUESTED DATA TO DATA CACHE MEMORY
596
DETERMINE WHICH CACHE LINE SHOULD BE REPLACED
594
IF WRITE-BACK READ OUT CACHE LINE FROM CACHE DATA MEMORY AND ISSUE STORE TO MEMORY CONTROLLER
598
WRITE REQUESTED DATA TO CACHE DATA MEMORY AND MODIFY TAG
602
END
608
RETURN DATA TO BUS MASTER
604
END
606

FIG. 20

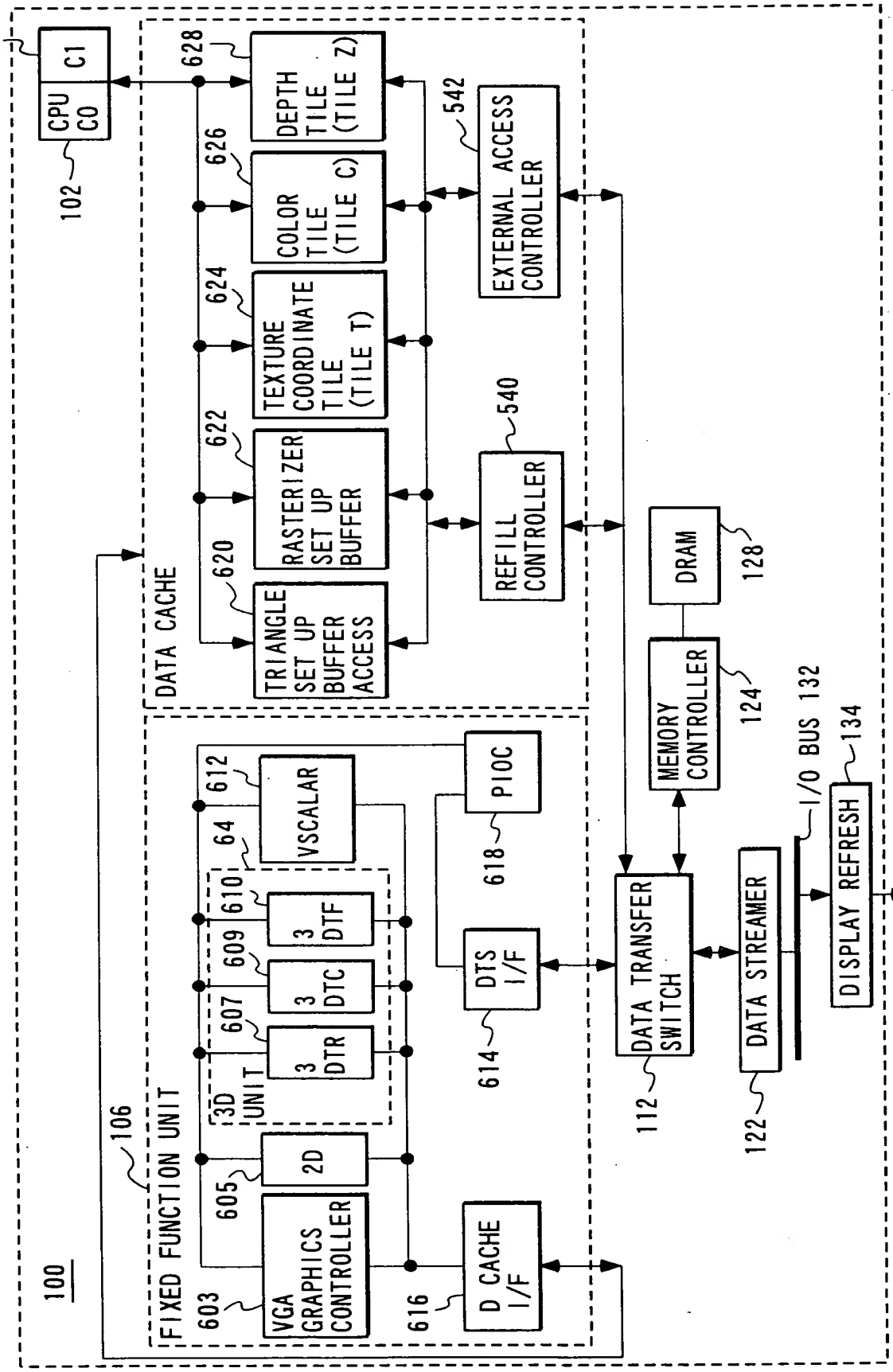

100
104
CPU C0
C1
102
DATA CACHE
628
DEPTH TILE (TILE Z)
626
COLOR TILE (TILE C)
624
TEXTURE COORDINATE TILE (TILE T)
622
RASTERIZER SET UP BUFFER
620
TRIANGLE SET UP BUFFER ACCESS
542
EXTERNAL ACCESS CONTROLLER
540
REFILL CONTROLLER
DRAM
128
MEMORY CONTROLLER
124
I/O BUS 132
DISPLAY REFRESH
134
DISPLAY
DATA TRANSFER SWITCH
112
DATA STREAMER
122
106
FIXED FUNCTION UNIT
612
VSCALAR
64
610
3 DTF
609
3 DTC
607
3 DTR
3D UNIT
605
2D
603
VGA GRAPHICS CONTROLLER
P10C
618
DTS I/F
614
D CACHE I/F
616

FIG. 21

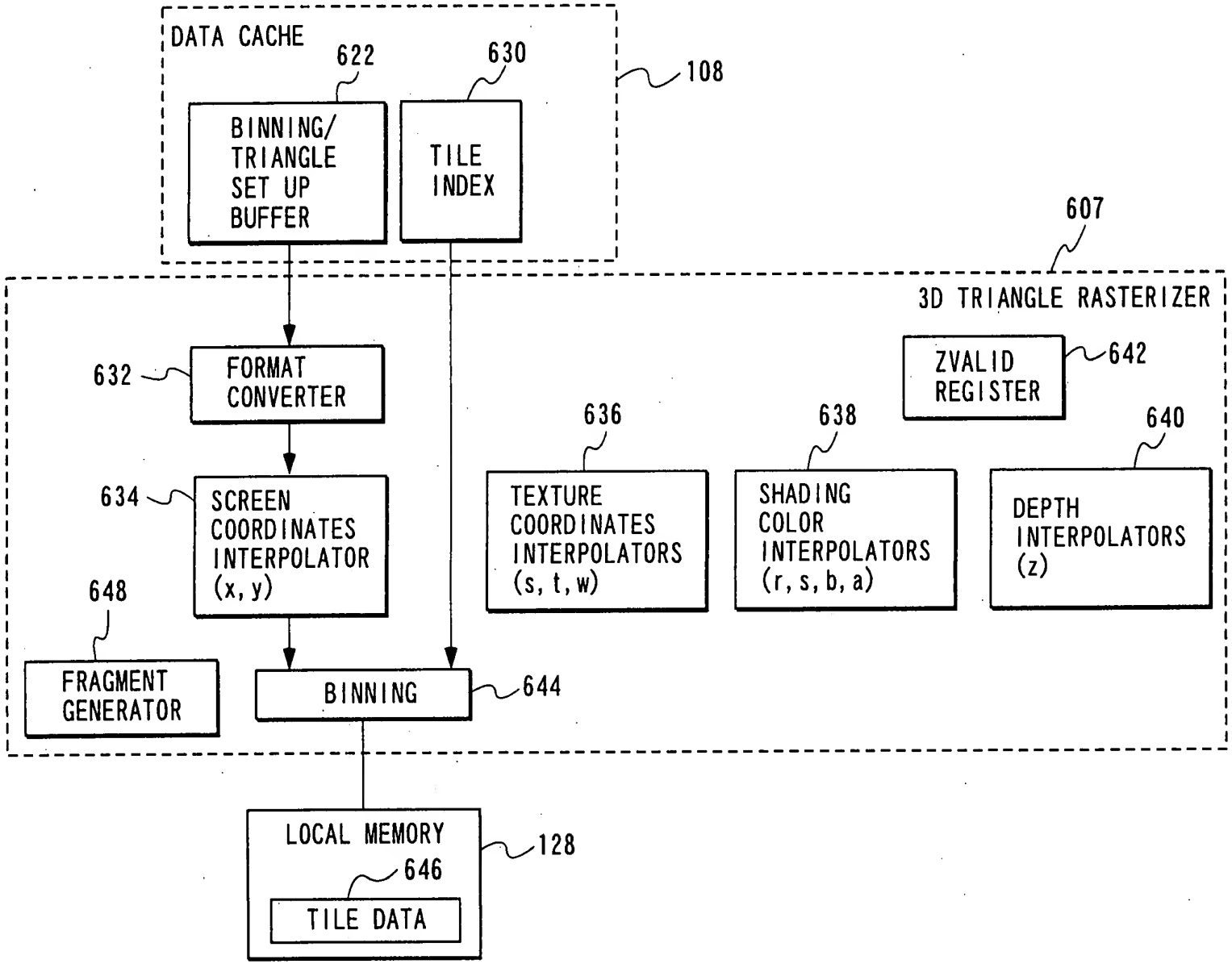

DATA CACHE
622
630
108
BINNING/
TRIANGLE
SET UP
BUFFER
TILE
INDEX
607
3D TRIANGLE RASTERIZER
632
FORMAT
CONVERTER
ZVALID
REGISTER
642
636
638
640
634
SCREEN
COORDINATES
INTERPOLATOR
(x, y)
TEXTURE
COORDINATES
INTERPOLATORS
(s, t, w)
SHADING
COLOR
INTERPOLATORS
(r, s, b, a)
DEPTH
INTERPOLATORS
(z)
648
FRAGMENT
GENERATOR
BINNING
644
LOCAL MEMORY
128
646
TILE DATA

FIG. 22

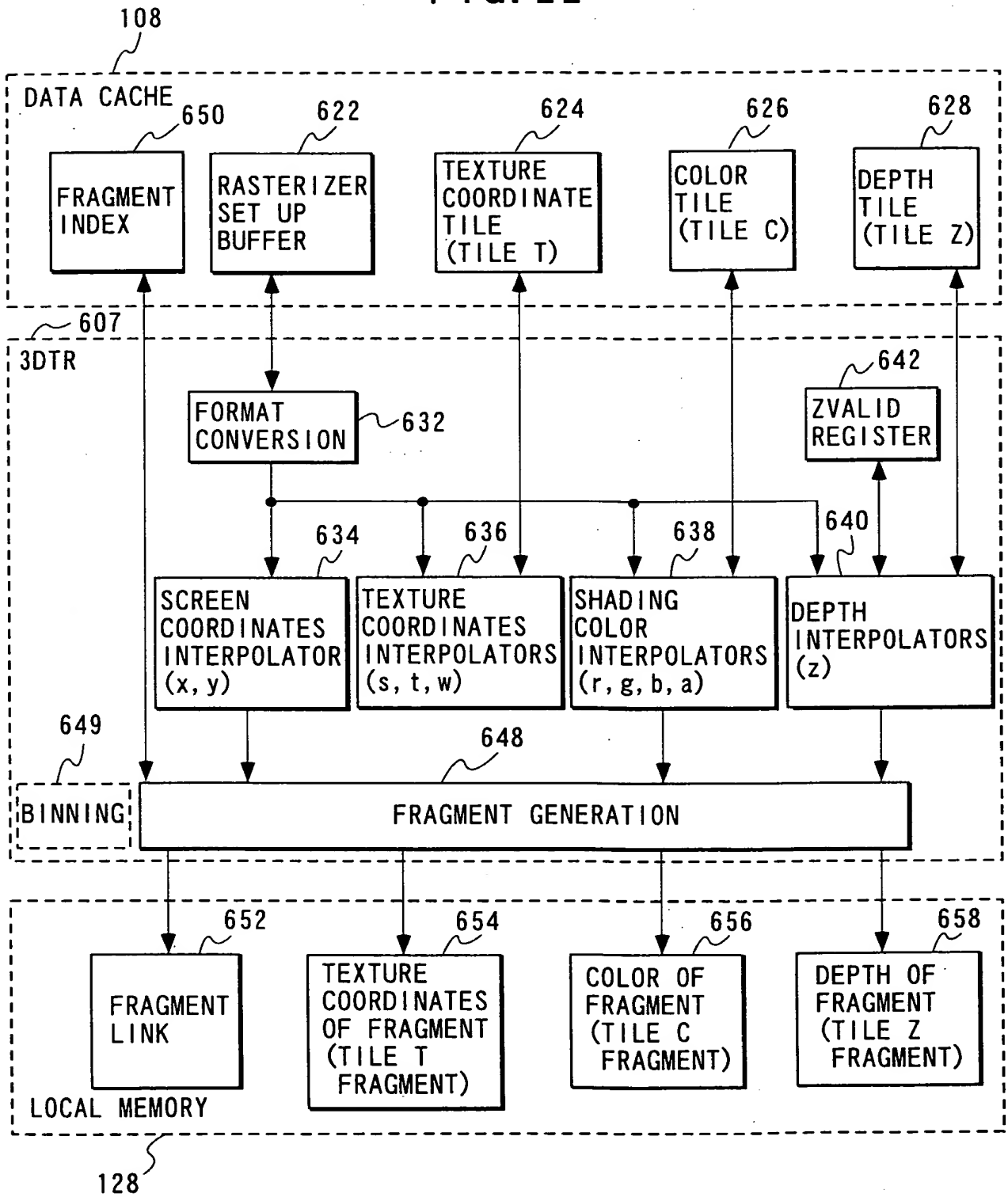


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FIG. 23

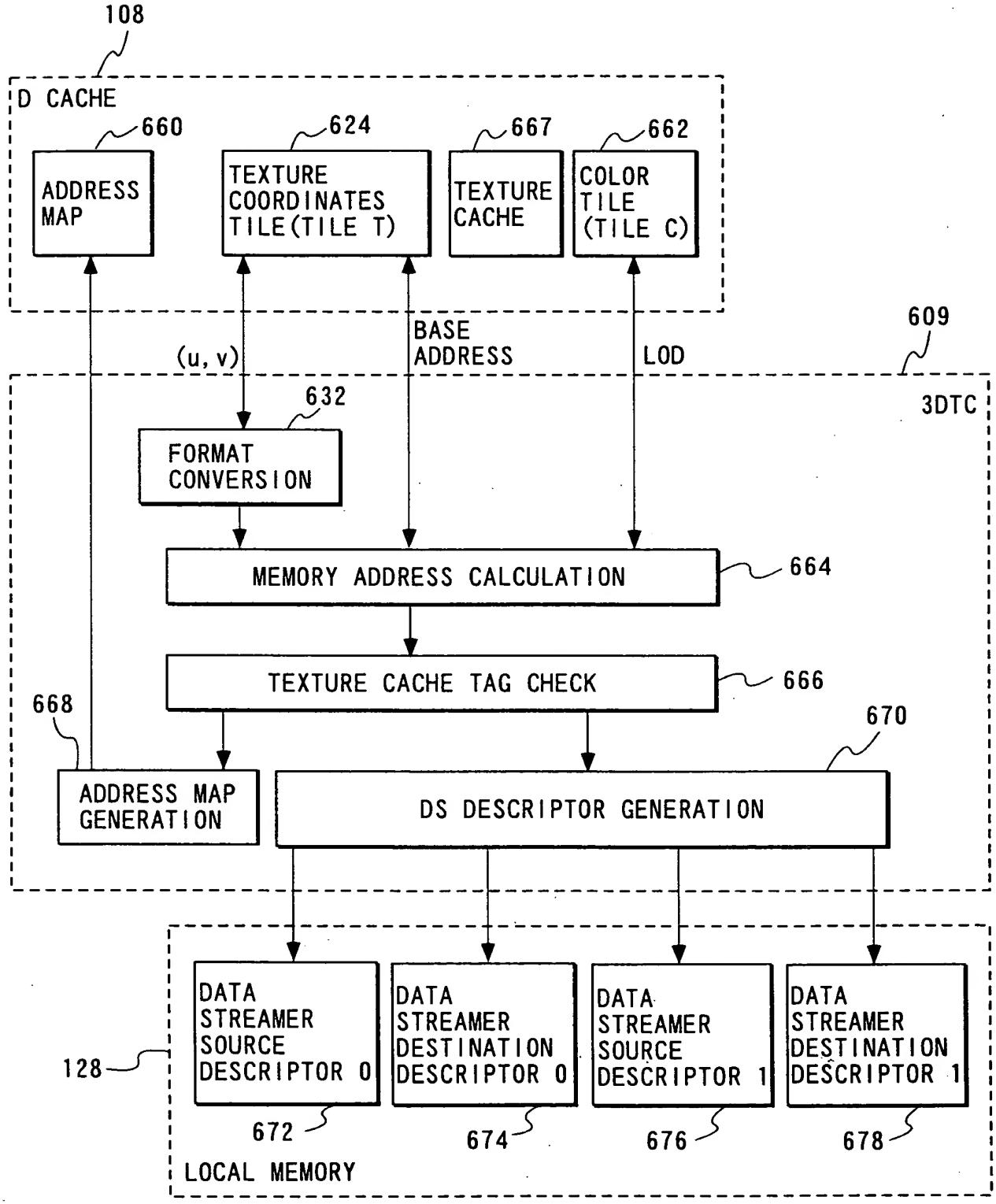

108
D CACHE
660
ADDRESS MAP
624
TEXTURE COORDINATES TILE(TILE T)
667
TEXTURE CACHE
662
COLOR TILE (TILE C)
609
(u, v)
BASE ADDRESS
LOD
3DTC
632
FORMAT CONVERSION
MEMORY ADDRESS CALCULATION
664
TEXTURE CACHE TAG CHECK
666
668
670
ADDRESS MAP GENERATION
DS DESCRIPTOR GENERATION
128
DATA STREAMER SOURCE DESCRIPTOR 0
DATA STREAMER DESTINATION DESCRIPTOR 0
DATA STREAMER SOURCE DESCRIPTOR 1
DATA STREAMER DESTINATION DESCRIPTOR 1
672
674
676
678
LOCAL MEMORY

FIG. 24

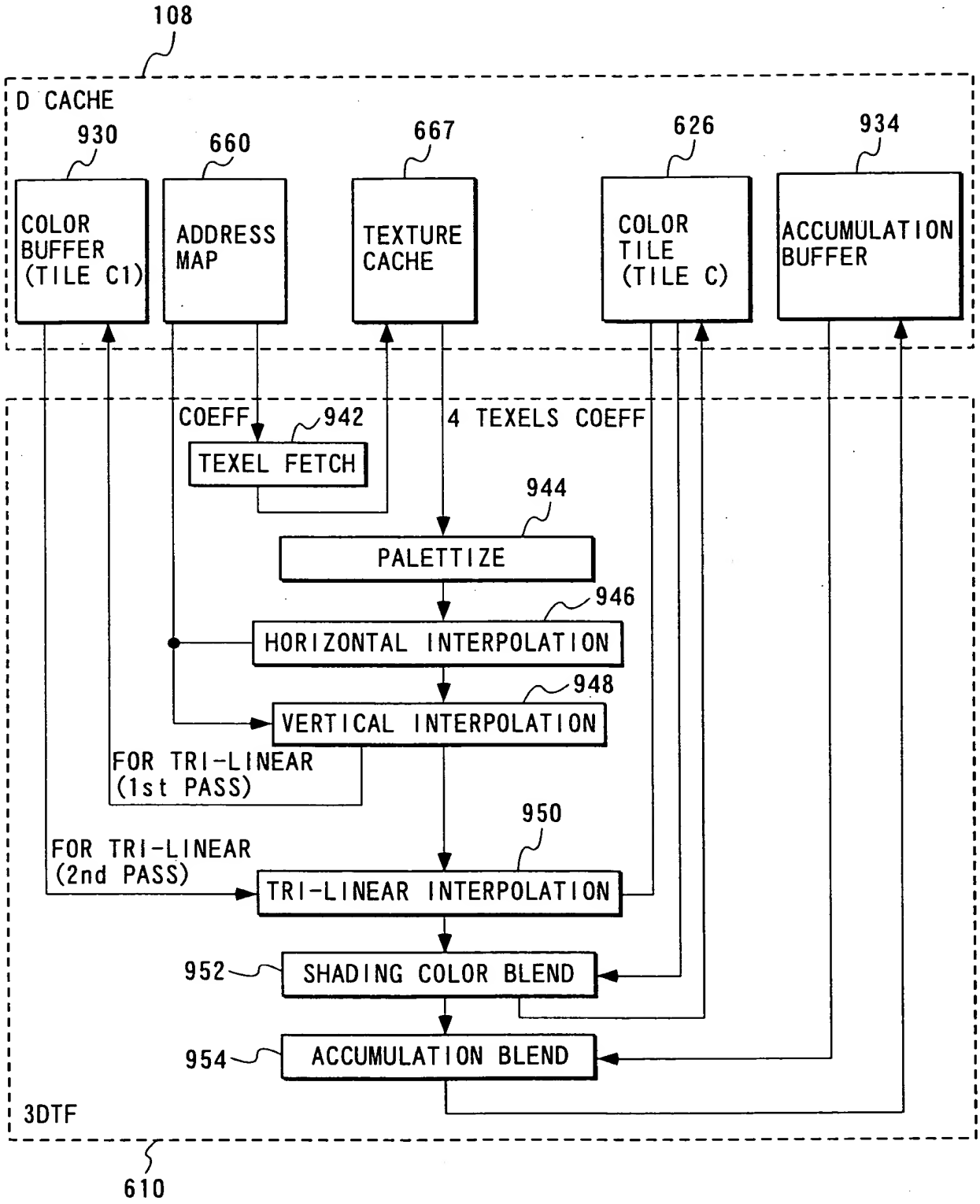

108
D CACHE
930
660
667
626
934
COLOR BUFFER (TILE C1)
ADDRESS MAP
TEXTURE CACHE
COLOR TILE (TILE C)
ACCUMULATION BUFFER
COEFF
942
4 TEXELS COEFF
TEXEL FETCH
944
PALETTIZE
946
HORIZONTAL INTERPOLATION
948
VERTICAL INTERPOLATION
FOR TRI-LINEAR (1st PASS)
950
FOR TRI-LINEAR (2nd PASS)
TRI-LINEAR INTERPOLATION
952
SHADING COLOR BLEND
954
ACCUMULATION BLEND
3DTF
610

FIG. 25A

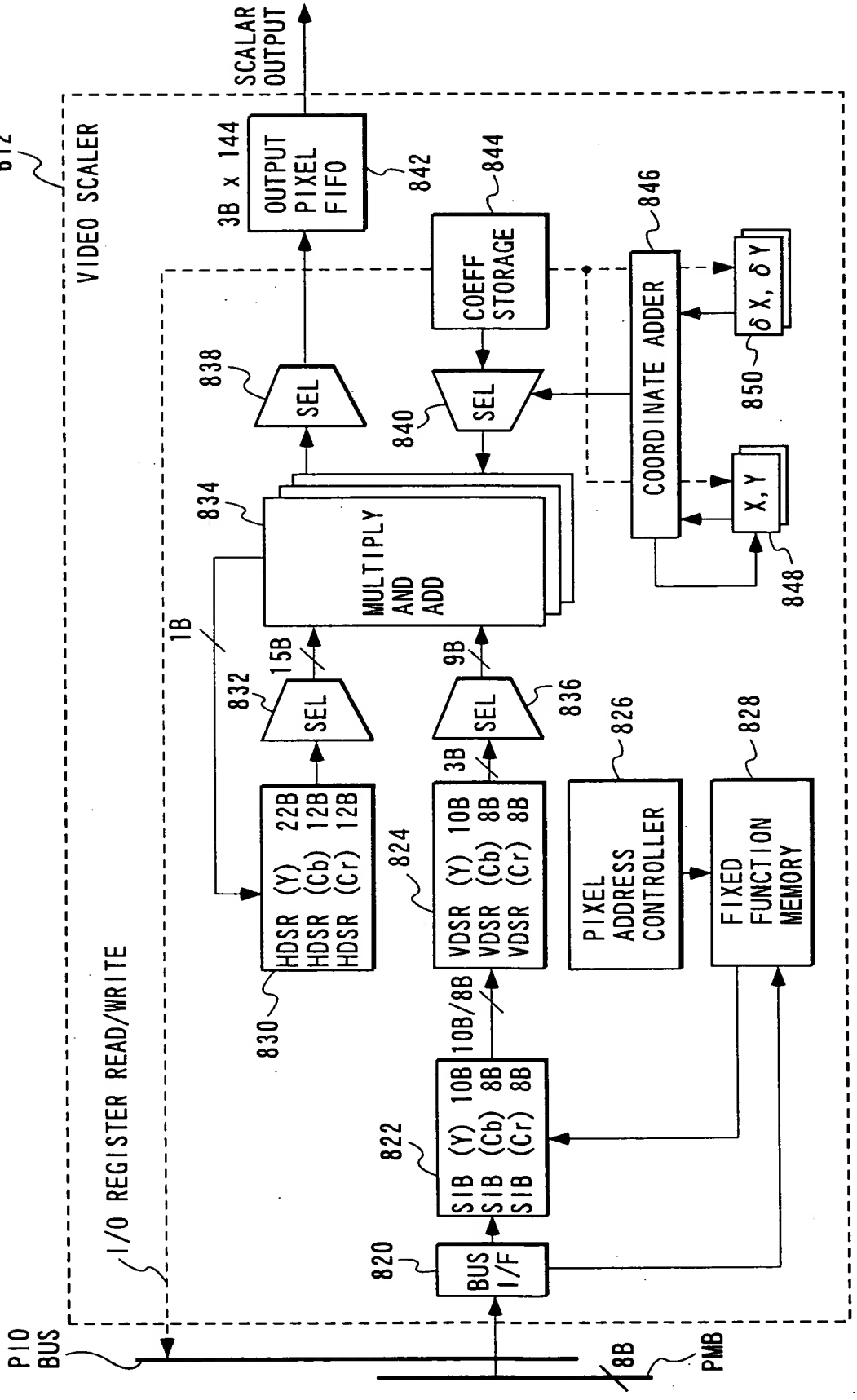

612
VIDEO SCALER
SCALAR OUTPUT
3B x 144
OUTPUT PIXEL FIFO
842
838
SEL
844
COEFF STORAGE
846
COORDINATE ADDER
δX, δY
850
840
SEL
834
MULTIPLY AND ADD
X, Y
848
1B
832
15B
SEL
9B
SEL
836
826
PIXEL ADDRESS CONTROLLER
828
FIXED FUNCTION MEMORY
HDSR (Y) 22B
HDSR (Cb) 12B
HDSR (Cr) 12B
830
824
VDSR (Y) 10B
VDSR (Cb) 8B
VDSR (Cr) 8B
3B
10B/8B
SIB (Y) 10B
SIB (Cb) 8B
SIB (Cr) 8B
822
820
BUS I/F
I/O REGISTER READ/WRITE
P10 BUS
8B
PMB

FIG. 25B

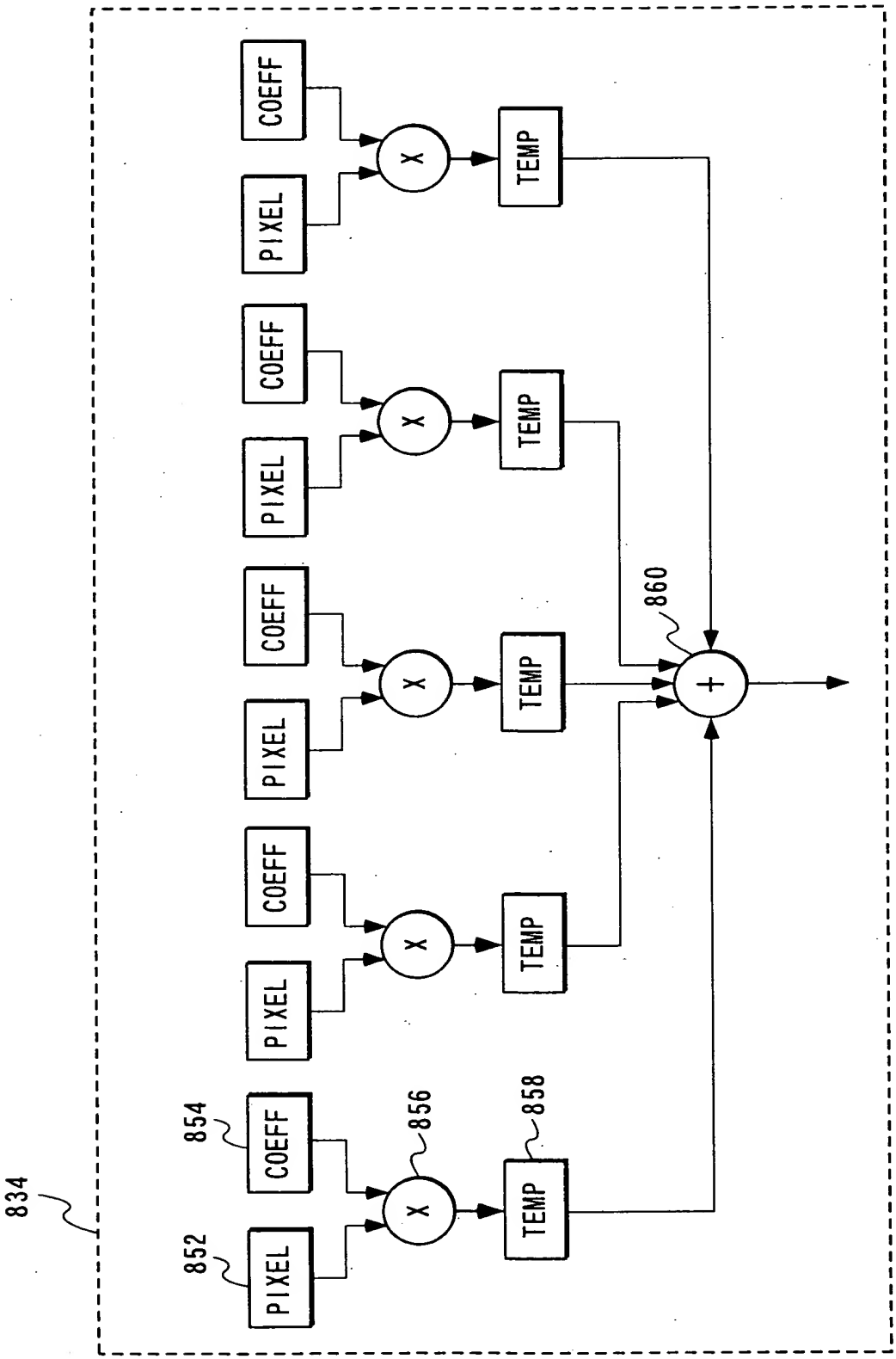
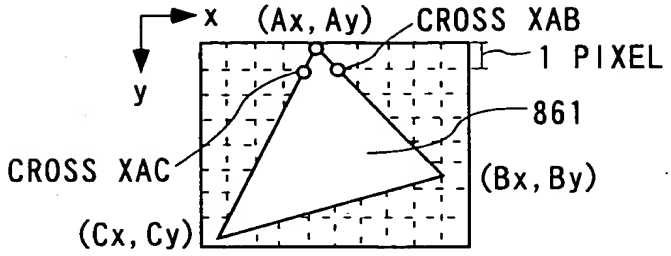
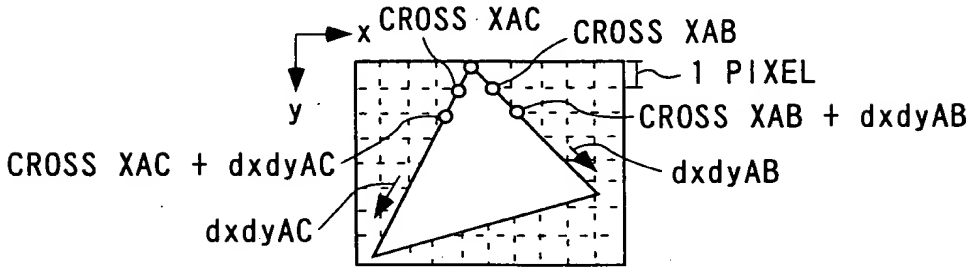


FIG. 26

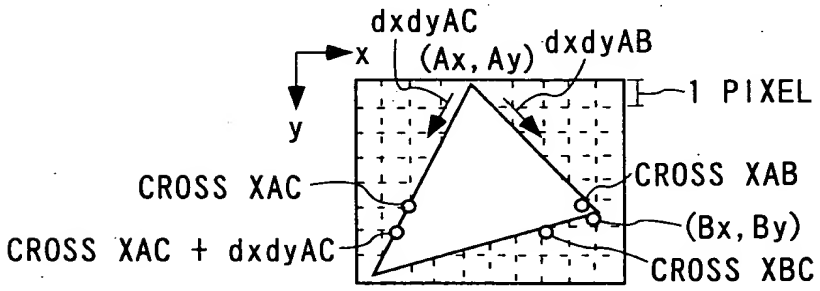
STEP 862



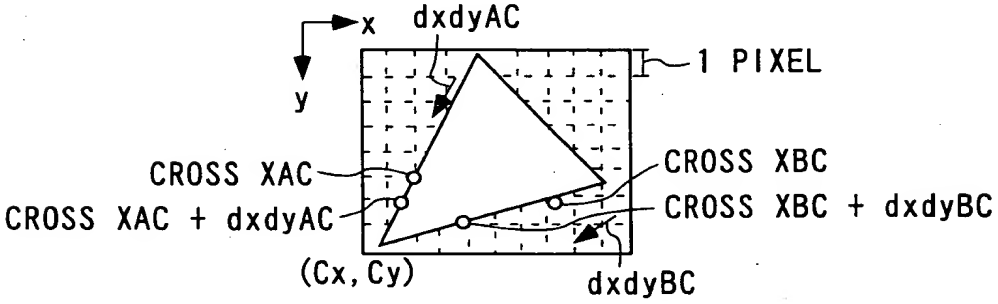
STEP 864



STEP 866



STEP 868



STEP 870

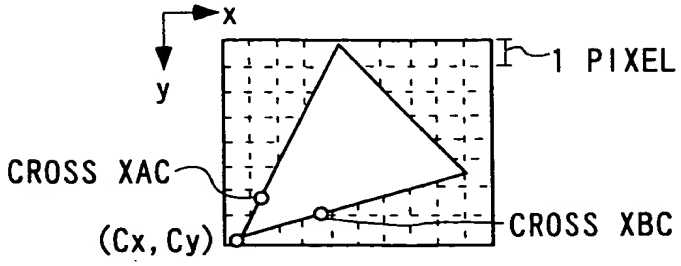


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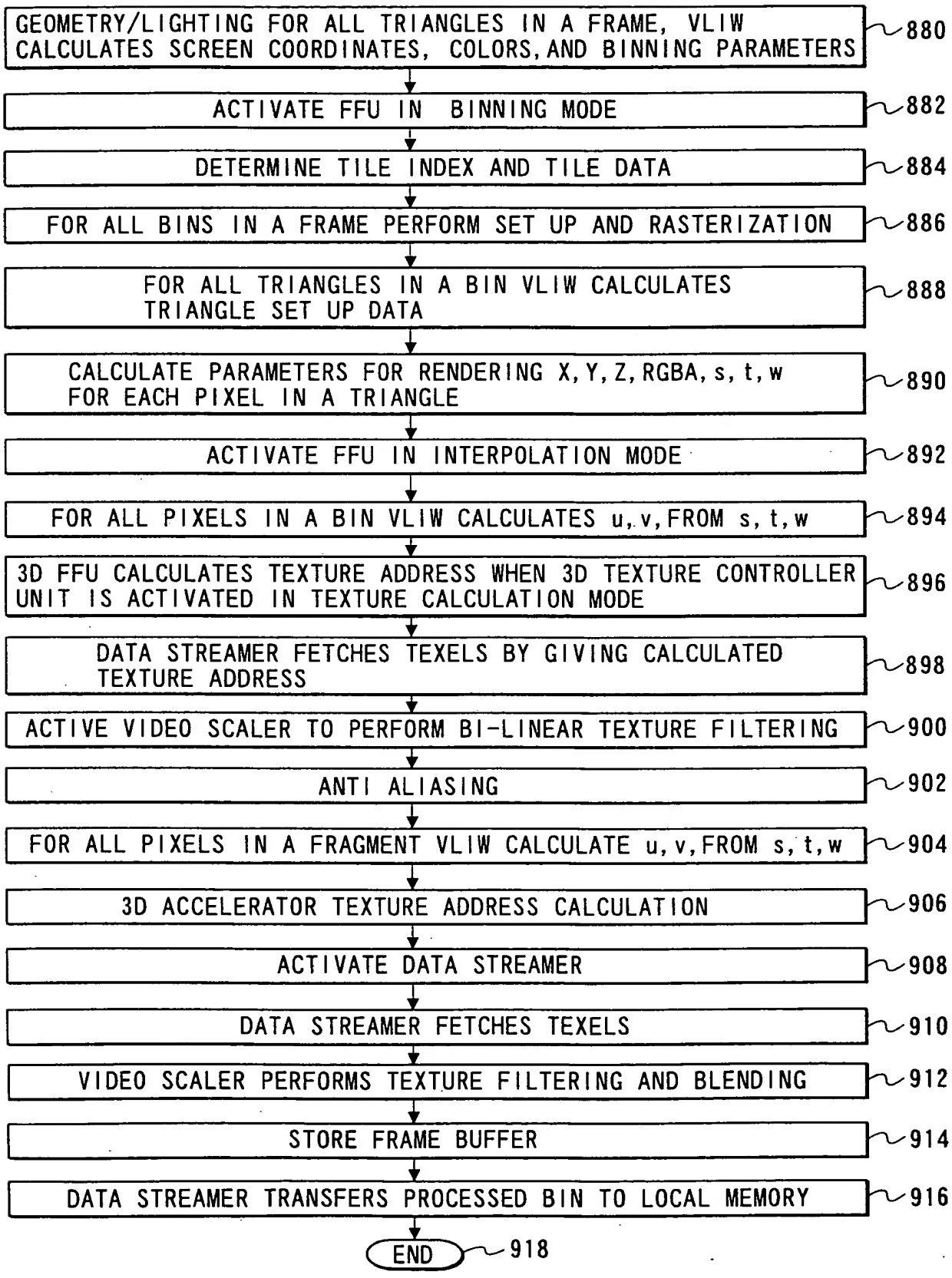
FIG. 27



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